Operating and Service Manual

DIGITAL STORAGE OSCILLOSCOPE

OS 4100

GOULD

An Electrical/Electronics Company

GOULD

MANUAL PART NO.
OS-804100

DIGITAL STORAGE OSCILLOSCOPE

OS 4100

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NOTE TO USER

This manual, the Digital Storage Oscilloscope OS4100 (PN OS-804100), replaces the Digital Storage Oscilloscope OS4100 Operator's Manual.

The manual contains expanded Circuit Description and Maintenance sections plus a Component List and Illustrations section which is new.

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Introduction

Section 1

The Gould OS4100 is a second generation Digital Storage Oscilloscope/Waveform Digitizer offering both T-Y and X-Y modes of operation. With a maximum A to D sampling rate of 1MHz, the 1k x 8-bit memory content is recalled to give a clear bright display on the 8 x 10cm electrostatically deflected CRT with 6kV overall accelerating potential and illuminated graticule.

Digital Storage offers many advantages over the more common tube storage: Pre-Trigger viewing, Indefinite storage time, Hard copy output, Flicker free low frequency performance, Channel 1 or 2 stored for comparison with Channel 1. Actual "X" expansion for detailed examination after capture, Ease of use and low cost of CRT.

A useable sensitivity of 100μV/cm is available on both "Y" channels with a switchable "Isolate" position avoiding the effects of Hum and Ground Loop problems. Other comprehensive signal conditioning and trigger facilities are offered including "Trigger window", which allows a transient moving in either a positive or negative direction to initiate a trigger.

The OS4100 has been designed for ease of use with all controls positioned for operator convenience. Great care has been taken with the mechanical construction to give reliability with ease of access, resulting in low cost of ownership backed by the traditional Gould 2 year warranty.

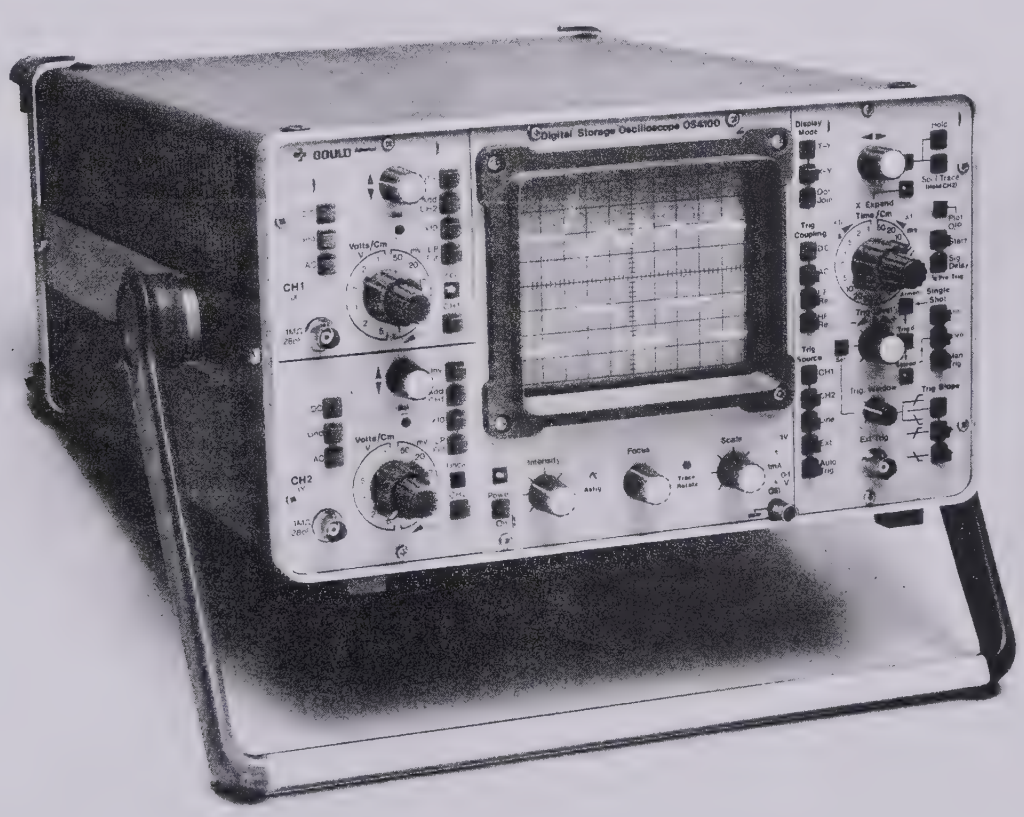


FIGURE 1-1 GOULD DIGITAL STORAGE OSCILLOSCOPE – OS4100

Specification

Section 2

DISPLAY

8 x 10cm rectangular CRT operating at 6kV.

Illuminated internal graticule.

VERTICAL DEFLECTION

Two identical input channels.

Sensitivity: 1mV/cm to 5V/cm in 12 ranges, X10 switch facility allows 100μV/cm. Uncalibrated fine gain control gives >2.5:1 reduction in sensitivity with UNCAL warning light.

Accuracy: ±3%.

Input Filter: H.F. rejection above approx. 10kHz.

Input Coupling: DC-GND-AC (−3dB at approx. 2Hz).

Input Impedance: 1MΩ/28pF.

Maximum Input: 400V D.C. or pk A.C.

Input Selection: Independently for each channel, on/off, invert and add-to-other-channel.

TIMEBASE

Ranges: 100μs/cm to 50s/cm in 18 ranges.

X Expand control allows variable expansion up to X10, post storage.

Accuracy: ±3% at X1 and X10 expansion.

DISPLAY MODES

T-Y: With CH1, CH2 or both displayed against selected timebase. (10cm x 8cm).

X-Y: CH1 and CH2 stored at the selected timebase rate with CH1 displayed against CH2. (8cm x 8cm.)

Dot Joining: Facility can be selected to avoid display confusion.

TRIGGER

Source: CH1, CH2, Line or External.

Coupling: D.C., A.C., H.F. Reject, L.F. Reject.

Slope: +, − or window mode.

Sensitivity: 2mm pk/pk to 1MHz internal.
100mV pk/pk to 1MHz external.

Level: Manual level control range approx. ±5cm internal
approx. ±1.0V external.
Manual window control range
approx. 0.5 to 6cm internal
approx. 0.1 to 1.2V external.

STORAGE MODES

Stored data and display normally updated to current input signals.

Single Shot: Retains next triggered sweep.

Hold: Freezes data immediately.

Split Trace: Retains alternate samples of stored data:-

i) In dual channel mode to retain CH2 only.

ii) In single channel mode to retain one trace superimposed on current input waveform.

Signal Delay: 25% trace length at all timebase sweep rates.

RESOLUTION

1MHz, 8 bit A/D converter with 1k store.

Vertical Resolution: Approx. 30 steps/cm.

Horizontal Resolution: Approx. 100 samples/cm at X1 expansion.
Approx. 10 samples/cm at X10 expansion.

Sampling Rate: 1MHz single channel at 100μs/cm. 500kHz dual channel at 100μs/cm reducing in proportion to timebase range. X to Y sampling time difference less then 2ps.

Bandwidth: −3dB amplitude response at approx. 600kHz.

ADDITIONAL FACILITIES

Calibrator: 1V pk/pk ±1% at 1kHz ±1%.

Isolation: Common mode input impedance (frame to supply ground) approx. 100k/500pF to approx. ±1V pk.

POWER

100, 120, 220, 240V ±10%
45 - 400Hz.
approx. 30VA.

Safety Class: IEC 348 Class 1.

TEMPERATURE RANGE

Operating: 0 to 50°C.

Full Specification: 15 to 35°C.

SIZE

178mm x 312mm x 417mm. (7" x 12 3/8" x 16 1/2")

WEIGHT

Approx. 10kg. (21.7 lbs.)

ACCESSORIES SUPPLIED

2 x Passive Probe Kits type PB12A
Power Cord

OPTION 4103

ANALOG OUTPUTS

CH1 AND CH2

Amplitude: 100mV/cm of screen height, bipolar with 0V corresponding to middle of screen.

Accuracy: Output voltage per cm of display ±3%
Output to input voltage (cal) ±3%

X RAMP

Amplitude: 100mV/cm of screen width, positive ramp resetting to 0V.

Accuracy: Output voltage/cm of display ±3%
Output voltage/unit time recorded ±3%

Time accuracy of Y Channel Outputs ±1% (record to replay ratio).

Output Impedance: CH1, CH2 and X ramp approx. 100Ω/ 0.1μF. Continuous short circuit protected.

READOUT RATE

Range: 20s/cm–5ms/cm in 1-2-5 steps.

Readout Bandwidth: DC–16kHz (–3dB).

CONTROLS

Plot Mode: Manual start (or remote), auto start or continuous read-out.

Start-up Delay: Delay between start command and initiation of read-out cycle, <100ms to >1sec. Range 100ms to 1s.

OUTPUTS

Contacts: Isolated single pole contact which closes from start command to end of read-out cycle.

Rating: 200V D.C., 0.5A D.C., 10W D.C.

Isolation: 400V max.

Plot Marker: T.T.L. high commencing at the end of the delay, for the duration of the read-out cycle.

3.1 POWER

FOR SAFETY, THE INSTRUMENT MUST BE GROUNDED VIA THE THREE CONDUCTOR POWER CORD.

THIS GROUND PATH MAY BE INTERRUPTED TO AVOID LOW LEVEL GROUND LOOP PICK UP PROBLEMS – SEE SECTION 3.8.

The instrument is normally shipped from the factory with the supply range switch on the rear panel set to the 100V (±10%) range. Check that this is correctly set to suit the local supply voltage before switching on. Note that the correct fuse for the two higher voltage ranges is 1 Amp Slo-Blo. (Gould Part No. AD-234790).

If the 220V or 240V ranges are to be used then a 1/2 Amp Slo-Blo fuse (Gould Part No. AD-233685) should be fitted.

CAUTION: DO NOT CHANGE THE SUPPLY RANGE SWITCH WITH THE INSTRUMENT CONNECTED TO THE POWER SOURCE.

While the instrument does not rely on forced air circulation, it should not be operated at elevated temperatures if the natural convection cooling is restricted, particularly at the rear of the instrument.

The instrument is switched on by pressing the POWER button when the associated indicator lamp should light.

3.2 CRT CONTROLS

These controls are grouped below the CRT display.

INTENSITY: This is used to set optimum trace intensity depending on ambient lighting conditions.

FOCUS: Used to obtain the finest possible trace width.

SCALE: The graticule is easily visible under normal lighting conditions. Graticule illumination is usually only required under low ambient light conditions or when photographically recording the display. The intensity required will depend on the film speed, aperture and exposure time being used.

ASTIGmatism: This control should rarely require readjustment once a setting is established. It is used in conjunction with the FOCUS control to obtain the finest trace in both horizontal and vertical directions.

TRACE ROTation: This control is used to ensure that the undeflected display is parallel to the horizontal graticule lines. It may require readjustment if the instrument is used in locations with a strong magnetic field.

3.3 Y CHANNEL CONTROLS

These controls are grouped to the left-hand side of the CRT display together with the CH1 and CH2 input sockets.

Note that the controls are arranged in two identical groups, upper and lower, corresponding to their respective BNC input socket. The selection of the input channel to be displayed is determined by the two push-buttons, CH1 and CH2. If both buttons are pressed, a dual trace display is obtained in the 'chop' mode, the switching frequency being equal to the sample rate (see Table 3-1). Note that when the X-Y display mode is selected (see Section 3.4) both channel select buttons must be pressed.

Input Coupling: For direct connection of the input signal, set the associated AC-GND-DC input switch to DC. For capacitive coupling of the input via an internal 0.1μF 400V capacitor, select the AC position.

NOTE: When examining low amplitude a.c. signals superimposed on a high d.c. level, AC coupling should be used and the sensitivity of the Y amplifier increased.

To locate the baseline, set the input coupling switch to the GND setting. In this position the input signal is removed from the amplifier and the amplifier input is grounded.

Sensitivity: Set the VOLTS/cm switch to a suitable position consistent with the amplitude of the input signal.

To obtain an input sensitivity in between those marked use the fine gain control which is concentric with the main VOLTS/cm switch. The fine gain control has a range of 3:1 so that its full adjustment overlaps the adjacent switched sensitivity ranges. Since the fine gain control is uncalibrated always ensure that the control is in the fully clockwise CAL position when making amplitude measurements. Whenever this control is moved away from the CAL position, an UNCAL warning indicator will be lit. At the CAL setting the input sensitivity corresponds to the setting of the VOLTS/cm switch.

X10

To increase the input sensitivity by a factor of ten, press the X10 button. This is effective on all VOLTS/cm ranges but the indicated setting should be divided by ten, i.e. the 1mV/cm range becomes 100μV/cm. See Section 3.8 for hazards encountered when examining very low amplitude input signals.

Shift

To position the trace in the vertical direction adjust the shift control (identified by vertical arrows).

BALance

The preset balance control should be adjusted to minimize vertical movement of the associated traces when the inputs are grounded and the X10 button is pressed with the VOLTS/cm switch set at 1mV/cm. This should only be done after a reasonable warm-up time of, say, 15 minutes and should only require infrequent adjustment thereafter.

L.P. FILTer
Pressing this button inserts a low pass filter into the amplifier path to provide attenuation of unwanted high frequency noise or interference when viewing low frequency signals. The filter has a −3dB cut-off frequency of approximately 10kHz and attenuates frequencies above this at the rate of 6dB/Octave or 20dB/Decade. The rise time of the amplifier is reduced to approximately 35μs when the filter is switched in.

TABLE 3.1 SAMPLE RATE & I/P FREQUENCIES

TIME/CM Range	Sample Rate		Maximum Input Frequency	
	Single Channel	Dual Channel or Split Track	Single Channel	Dual Channel or Split Track
0.1ms/cm	1MHz	500kHz	200kHz	100kHz
0.2ms/cm	500kHz	250kHz	100kHz	50kHz
0.5ms/cm	200kHz	100kHz	40kHz	20kHz
1ms/cm	100kHz	50kHz	20kHz	10kHz
2ms/cm	50kHz	25kHz	10kHz	5kHz
5ms/cm	20kHz	10kHz	4kHz	2kHz
10ms/cm	10kHz	5kHz	2kHz	1kHz
20ms/cm	5kHz	2.5kHz	1kHz	500Hz
50ms/cm	2kHz	1kHz	400Hz	200Hz
0.1sec/cm	1kHz	500Hz	200Hz	100Hz
0.2sec/cm	500Hz	250Hz	100Hz	50Hz
0.5sec/cm	200Hz	100Hz	40Hz	20Hz
1sec/cm	100Hz	50Hz	20Hz	10Hz
2sec/cm	50Hz	25Hz	10Hz	5Hz
5sec/cm	20Hz	10Hz	4Hz	2Hz
10sec/cm	10Hz	5Hz	2Hz	1Hz
20sec/cm	5Hz	2.5Hz	1Hz	0.5Hz
50sec/cm	2Hz	1Hz	0.4Hz	0.2Hz

ADD CH2 (CH1)
Pressing this button adds a signal from the other input channel to the original signal. The calibration of the added signal is determined by the VOLT/cm switch of the channel to which the signal is applied but is unaffected by either of the fine gain controls.

INVert
Pressing this button inverts the displayed signal.
Note that this inversion operates only on an input signal applied directly to the input socket of that channel and not on a signal added from the other channel by means of the ADD button.

For example, if on the CH2 controls both the ADD CH1 and INV buttons are pressed, the signal displayed is CH1−CH2. Operation of the CH2 fine gain control affects only the CH2 signal allowing an accurately balanced difference signal to be displayed. Releasing the INV button causes the CH1 + CH2 signal to be displayed. Note that the vertical position of this composite signal is affected by the CH2 shift control only.

With either channel set for sum or difference mode, both channels can remain selected for dual channel display. This flexibility allows one channel to be shown with the sum or difference, or the sum to be shown with the difference.

3.4 TIMEBASE AND TRIGGER CONTROLS

All the controls associated with the timebase, trigger and display mode are grouped to the right hand side of the C.R.T. display.

X Shift
This control (identified by horizontal arrows) positions the trace in the horizontal direction. Note that both coarse and fine controls are combined: the main coarse control has a 60° backlash zone in which only the fine control operates.

Timebase Sweep Speed
The timebase sweep speed (i.e. the time scale of the horizontal axis) is set by the TIME/cm control. Note that the indicated speeds are only correct when the X EXPAND control is in the X1 position.

X EXPAND
This control is concentric with the TIME/cm knob and provides magnification of the display in the horizontal axis. Use with the X shift control allows detailed examination of any particular part of the trace. Calibrated expansion positions of X1 and X10 are provided at the fully anti-clockwise and fully clockwise extremes of the control range respectively, with a continuously variable degree of expansion obtainable at intermediate settings. Since the TIME/cm markings are only correct with the X EXPAND control in the X1 position an indicator lamp provides visible warning whenever the expansion control is moved away from this setting. With the control in the X10 position, indicated values of TIME/cm should be divided by ten when measuring time (i.e. 0.1ms/cm range becomes 10μs/cm.

TRIGger SOURCE
This group of switches selects the source of trigger signals: internal CH1, internal CH2, line (supply frequency) or an external signal applied to the EXTERNAL TRIGger BNC socket.

AUTO TRIGger
Also grouped with the TRIG. SOURCE switches is the AUTO TRIGger control. When this button is pressed the timebase is made to free run in the absence of trigger signals faster than approximately 10Hz. This facilitates positioning of baselines etc., in the absence of an applied signal. If the timebase is being triggered at a rate greater than 10Hz the control has no effect. For viewing signals with a repetition rate less than 10Hz or for transient signals the button should be released. Note that the SINGLE SHOT store and HOLD controls both override the AUTO TRIGger.

TRIGger COUPLING
This group of buttons selects the coupling mode of the trigger signal to the timebase. The DC position provides direct coupling and allows the instrument to trigger at a specific voltage level. AC coupling removes d.c. and

very slow a.c. components below 1.5Hz from the trigger signal. The LF REJect position provides a.c. coupling with a low frequency cut-off point of approximately 1.6kHz. This can be used to reduce the sensitivity of the trigger point to spurious low frequency signals such as 50/60Hz supply interference. The HF REJect button may be selected in addition to any of the other coupling functions to decrease trigger sensitivity at frequencies above 1.6kHz.

TRIGger LEVEL
The TRIGger LEVEL control selects the point on the displayed waveform (or external trigger input waveform) at which the timebase starts a sweep. Whenever an appropriate trigger signal is detected the TRIGgered indicator lamp will flash.

TRIGger SLOPE
This group of buttons selects the correct slope of the incoming trigger source signal, positive going or negative going, on which a sweep is initiated. The ± position may be selected in applications where it is desirable to trigger on either trigger slope (e.g. for capturing transients) and is used in conjunction with the TRIGger WINDOW control.

TRIGger WINDOW
This control becomes effective only when the ± position is selected at the TRIGger SLOPE controls. In this mode two independent trigger levels are established symmetrically spaced above and below the mean trigger level set by the main TRIGger LEVEL control. A sweep will be initiated whenever the incoming trigger signal goes outside the window, i.e. crosses the upper level in a positive going direction or the lower level in a negative going direction (see Fig. 1). The spacing between upper and lower threshold levels is set in the range of 0.5–6cm, (internal trigger) or 0.1–1.2 volts (external trigger) by the TRIGger WINDOW control and the mean (mid point) of the two thresholds is set by the main TRIGger LEVEL control. To ensure that the two levels enclose the quiescent signal, a SET indicator lamp is provided which is illuminated only when the input signal is between the upper and lower threshold levels. The TRIGger WINDOW control may then be used as a trigger sensitivity control to ensure that whenever the input signal deviates from its quiescent level by more than a pre-determined amplitude, a sweep is initiated and stored.

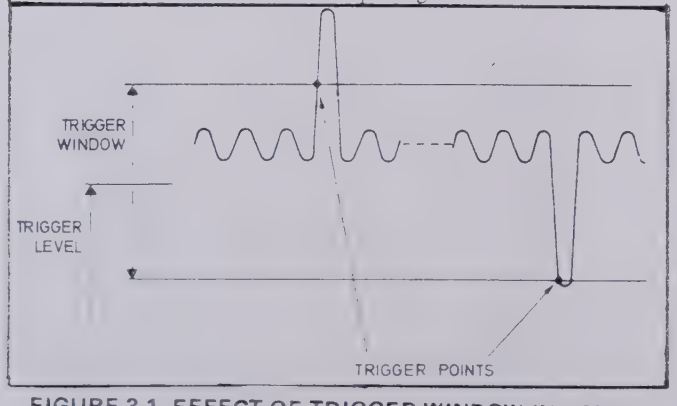


FIGURE 3-1 EFFECT OF TRIGGER WINDOW IN ± MODE

3.5 STORE CONTROLS

Introduction

In order to appreciate the full advantages of this digital storage oscilloscope it is helpful to understand the basic method of operation. For a more comprehensive description of the system employed refer to Section 4, but the brief description outlined below will serve to obtain the maximum benefit from the highly versatile store controls described in this section.

In a conventional dual trace oscilloscope, the two input signals are amplified by two identical pre-amplifiers and then multiplexed, in either a "chopped" or "alternate" mode, into a common output stage and applied to the vertical deflection plates of a C.R.T. display. A timebase ramp generator can be triggered either by a selected internal signal, or by some externally applied input, to provide a horizontal sweep at an appropriate speed.

In the OS4100, the two external signals are amplified by conventional pre-amplifiers, but are then presented to an analogue to digital converter. This samples the signals and produces an 8 bit digital code representing the magnitude of each of these samples. A train of 1024 such samples can, in digital format, be stored indefinitely in a solid state memory incorporated within the instrument. This information can then be re-called, non-destructively and repetitively, from the memory and displayed on the C.R.T. at a convenient, flicker free, rate.

In order to initiate this recording process, a conventional trigger system is incorporated which has all the comprehensive and flexible facilities commonly found on modern high grade oscilloscopes. When a trigger is received the instrument will enter a series of 1024 consecutive samples into the memory, automatically erasing the previously stored values. This new information will remain in the memory, and is continuously displayed on the C.R.T. until a further valid trigger signal is received. Note that the effective calibration in the horizontal (time) axis is simple determined by the intervals at which the input signals are sampled and stored and this may be varied over a wide range.

Once a signal has been stored in the memory it may be displayed in a variety of ways without altering the information in any way. Both input signals may be displayed against a time axis and may be expanded and shifted to aid examination. Alternatively one input signal may be plotted against the other as an X-Y display (see Section 3.6). With the addition of an output unit option the input signals may be transferred to a pen recorder or used as a signal source for external equipment (see Section 3.9).

HOLD
Pressing this button freezes the trace immediately and lights the associated indicator lamp. This control overrides all other store controls and provides failsafe reten-

tion of a particular display. Note this control may freeze the display mid way through an input sweep; to ensure that a complete sweep is retained use the SINGLE SHOT store sequence described below.

SPLIT TRACE (HOLD CH2)
This control has a dual function; when pressed with the instrument in a dual trace mode it freezes the CH2 trace only. When pressed in the single trace mode it freezes alternate samples of the current display so that a new input signal may be displayed with the remaining input samples and a comparison made between the two displays. This allows 'before' and 'after' signals to be displayed simultaneously. Pressing this button also bring on the HOLD indicator lamp to denote that part of the display is locked.

START PLOT O/P
This control is relevant only when the 4103 Output Unit option is fitted. See Section 3.9 for full operating details.

SIGnal DELAY
Pressing this button effectively inserts a signal delay into the signal path prior to the trigger pick-off. Thus it is similar to the signal delay sometimes fitted to conventional oscilloscopes except that the delay time increases as the timebase speed is reduced so that on X1 expansion, the visible delay is always equal to 2.5cms multiplied by the TIME/cm setting in use. Inserting signal delay whilst a repetitive signal is being displayed will cause the display to shift 2.5cms to the right so that 2.5cms of pre-trigger information becomes visible at the left hand side of the trace. This pre-trigger information is, of course, also available when viewing transient signals.

Note that if the signal delay is in use while the TIME/cm switch is set to the lower ranges, say below 0.2sec/cm, there will be a noticeable time lag between the adjustment of any Y amplifier controls – Y shift for example – and the corresponding change appearing on the displayed trace. Therefore it is recommended that positioning of baselines etc., is performed with the signal delay switched out (i.e. button released).

SINGLE SHOT
This group of three buttons controls the single shot store cycle. Pressing the ARM button retains any sweep in progress, or the next complete sweep initiated by a trigger as a stored display, unaffected by subsequent trigger signals. Three indicator lamps show the current status in the single shot cycle: the ARMED lamp indicates that the timebase has been primed by pressing the ARM button and is awaiting a valid trigger signal. When a trigger signal occurs the TRIG'D lamp comes on in place of the Armed lamp, and when the sweep is completed, the STORED lamp comes on. To repeat the sequence with a further single sweep, the ARM button should be pressed again. To return to the normal continuously triggered mode of operation, press the NORMAL button. If it is required to record a single sweep without using a synchronous trigger signal, the MANual TRIGger button may be pressed to generate an internal trigger signal.

Note that once the ARM button is pressed and the timebase enters the single shot mode, the AUTO TRIGger facility is automatically inhibited until the NORMAL button is pressed.

3.6 DISPLAY MODE

Two display modes are available: T-Y and X-Y.

These are selected by a group of buttons marked DISPLAY MODE. An additional button controls the dot joining. Dot joining should normally be selected except when the X-Y display mode is used with very slow sample rates (see below). Further information on the use of dot joining is given in Section 3.7.

T-Y MODE
With T-Y mode selected, the CH1 and CH2 signal inputs, as selected, are displayed as a vertical deflection against a horizontal axis representing time. The maximum display area available in the T-Y mode is 8.5cm (vertical) x 10.2cm (horizontal), adequately covering the 8cm x 10cm calibrated graticule area. Note that the vertical display area is restricted to 8.5cm by the analogue to digital convertor (see Section 4 for more details) and the trace cannot be deflected outside this area. The horizontal scan of 10.2cm may be positioned relative to the graticule area with the X shift control and may be increased up to X10 by using the X expansion control. The X shift and expansion controls are post storage controls and thus may be used with any signals displayed in the T-Y mode whether stored or not. The Y shift controls, however, operate prior to storage and once a trace has been stored, its vertical position may not be changed.

X-Y MODE: Display Format
In the X-Y mode, the CH2 input signal is displayed as a vertical deflection, as for T-Y, but the CH1 input signal is displayed as a horizontal deflection so that a plot of CH1 versus CH2 may be obtained. Thus CH1 and CH2 must be selected. In order to retain the calibration of the display relative to the CH1 VOLTS/cm setting, the display area in the X-Y mode is restricted to 8.5cm x 8.5cm symmetrical about the centre of the graticule. Both the X expansion and X shift controls are disabled in the X-Y mode; positioning of the display in the horizontal direction must be performed prior to storage with the CH1 shift control.

X-Y MODE: Sampling Rate Considerations
It should be noted that the choice of T-Y or X-Y mode affects the method of displaying the recorded input signal only. The technique of recording the input signals is identical for both (dual trace) T-Y mode and X-Y mode and once a signal has been stored it is possible to switch between the two display modes as desired.

In order to determine a suitable sampling rate or timebase range for a given application it should be remembered that since the trace length in the T-Y mode is 10.2cms, the total recording time available will be

approximately 10 times the setting on the TIME/cm control. Thus for an event lasting 18ms, the most suitable timebase range would be 2ms/cm. To ensure that a suitable timebase range has been chosen for a particular application, it is sometimes helpful to observe the input signals initially in the T-Y mode and then switch to the X-Y mode when the signal has been safely recorded. Note that if the signal delay is in use, ¼ of the available recording time will be storing events happening prior to the trigger signal and only ¾ of the time will be available after trigger.

The trigger controls are unaffected by the choice of display modes and should be adjusted in the same manner as for a T-Y display. If a snychronized trigger source is not available and the event to be recorded is repetitive in nature, the MANual TRIGger button may be used to initiate a recording sweep.

For repetitive signals, NORMAL rather than SINGLE SHOT trigger mode can be used to obtain a continuously updated X-Y display. In this mode, it is not necessary to retain trigger as data entry may free run in the AUTO mode.

An alternative technique is also possible if dot joining is not necessary, signals are repetitive and T-Y information is not required. Since samples of both display axis will be stored in the X-Y mode, it is not essential that these samples be taken in any historical order. Thus if the sample rate is set to a low value (i.e. the TIME/cm control set to a slow rate), X and Y co-ordinate pairs will be recorded in a psuedo-random manner. Dot joining should not be used with this recording technique since this will join the displayed points in the order in which they were recorded, which is not necessarily sequential. There is no advantage in using a synchronous trigger signal with this technique and the MANual TRIGger button may be used to commence recording.

X-Y Mode: X/Y Phase Shift Considerations

Since the instrument has only a single analog to digital converter it is not possible to record both X and Y co-ordinates at an identical instant of time. There is a time delay of up to 2μsec between the recording of sample points in each axis (regardless of TIME/cm control setting) and this will give apparent phase errors between X and Y as the signal frequencies are increased. In general, for small signal amplitudes, say of 2cm total amplitude in either axis, the distortions due to this effect will become noticeable (i.e. equivalent to a phase error of 3°) when the input signals, or a significant component of the input signals, exceeds a frequency of 5kHz, if the full 8cm display area is used these effects may be noticeable at input frequencies of 1kHz. While the instrument is capable of reproducing frequencies well in excess of these quoted figures, the effect of these phase errors should be allowed for if it is proposed to make accurate phase measurements at higher frequencies.

The differential time delay between corresponding X and Y samples is independent of the TIME/cm setting but is a function of X and Y deflection. The effective phase shift or trace distortion increases from top left of the screen to a maximum at the bottom right.

3.7 ALIAS EFFECTS

The OS4100 uses a sampling system to examine the incoming waveform. Any such system can give misleading results known as alias effects if the input signal has a significant component with a frequency approaching or above the sampling frequency.

Figure 3-2 shows the effect of the sampling process on a triangular input waveform (trace A). Trace B shows the effect of sampling at a frequency close to four times that of the input if the display is formed by a series of dots. This may be taken as meaningless information. Trace C shows the same signal as trace B, but with dot joining in operation so that the display is formed by a series of straight lines joining successive sampled levels. The dot joining approach is seen to retain the essential nature of the input waveform without ambiquity. This is particularly important since, in practice, the horizontal dot density is much closer than that shown on the diagram.

Waveform distortion is noticeable on trace C and this is a function of the sampling rate. If the sampling rate is reduced further, as in trace D where the sampling rate is close to twice the input frequency, the essential nature of the waveform will be lost. Trace E shows the display obtained when the sampling frequency is very nearly equal to the input frequency. The trace obtained shows the correct waveform but at a false frequency. This frequency division effect is true aliasing and is the principle on which high frequency sampling oscilloscopes operate, but can cause confusion in this case.

Clearly the minimum sampling rate necessary to examine a particular input waveform will be to some extent dependent upon the degree of waveform fidelity required. Table 1 lists the sampling rates obtained on different timebase ranges together with a recommended maximum input frequency based on 4 to 5 samples per cycle of input signal. The instrument will, however, indicate the presence of input frequency components above this recommended limit. Conversely, for applications where waveform distortion is critical, the timebase speed, and hence sampling rate, should be increased above that shown in the table.

If alias effects are suspected, it is recommended that the fastest possible sweep speed is selected. It should be noted that the sampling system will not reliably detect narrow transients unless the time duration of these transients is greater than the reciprocal of the sampling rate.

3.8 INSPECTION OF VERY LOW AMPLITUDE SIGNALS

The instrument is capable of recording and displaying input signals of very low amplitude, such as those commonly encountered with industrial, scientific and

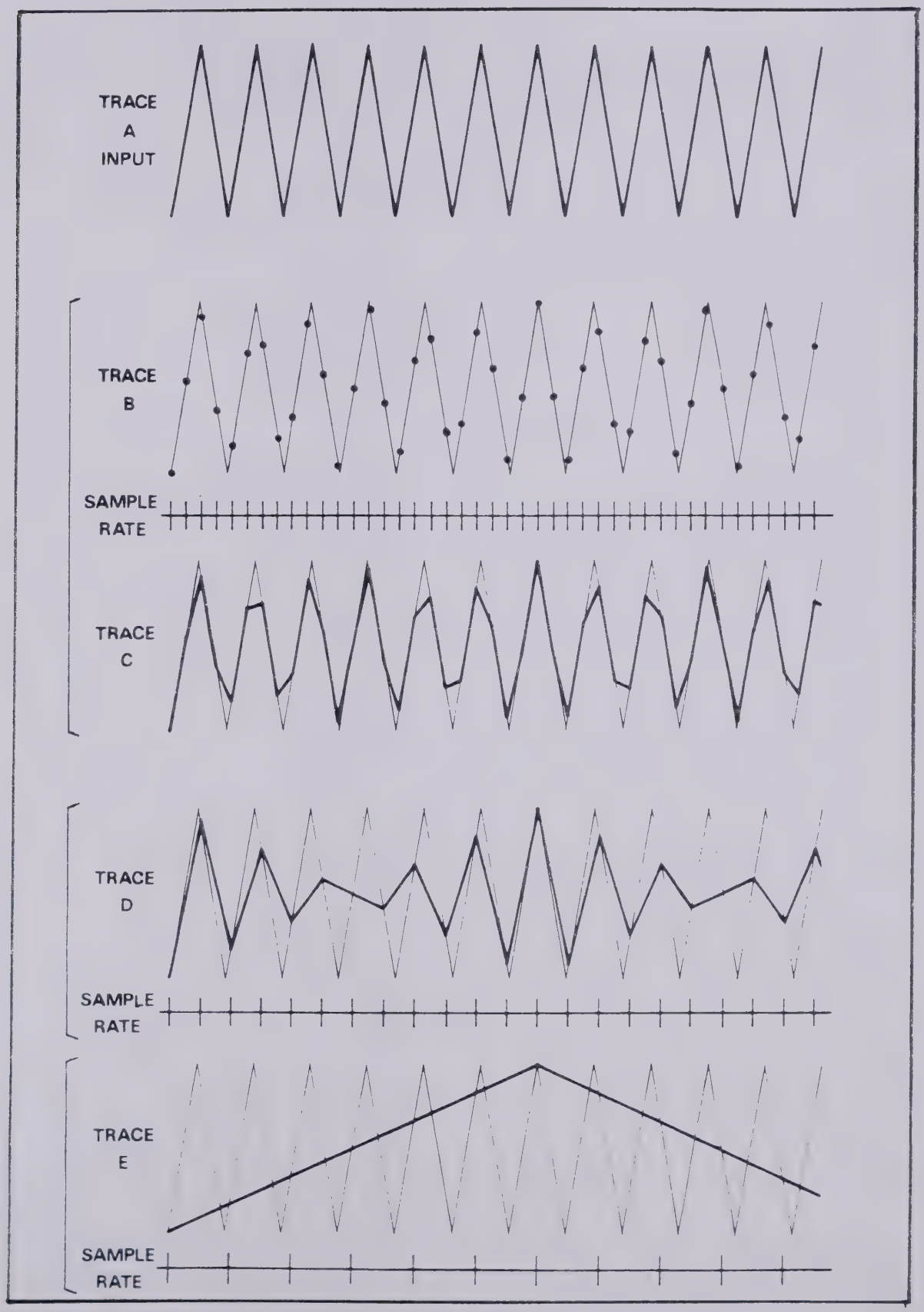


FIGURE 3-2 ALIAS EFFECTS

medical transducers. Some caution should be exercised, however, when measuring such signals, to ensure that externally impressed interference and background noise are minimised.

Input Noise

With the instrument in its most sensitive input setting of 100μV/cm a certain amount of random noise will be observed. This is largely due to the inevitable thermal noise generated by the high value (1M ohm) input resistors of the amplifiers plus a small amount due to the F.E.T. input amplifiers.

Both these effects can be minimised by providing the lowest possible signal source impedance to the instrument. The use of X10 passive divider probes at these low signal levels is definitely not recommended unless absolutely necessary since this will present a minimum 10M ohms source impedance.

Hum Loops and Ground Lead Interference

With any grounded equipment there exists the possibility of hum loops and ground lead interference caused by heavy currents flowing via the instrument to ground usually from external equipment connected to the instrument. This can be minimized on the OS4100 by setting the ground switch on the rear panel of the instrument to the 'ISOLATED' position. In this position the metal frame of the instrument is still grounded for safety purposes but via a diode isolation network (see Fig. 3-3) which allows both the frame and input low terminals to 'float' relative to the supply ground by approximately ±1 volt.

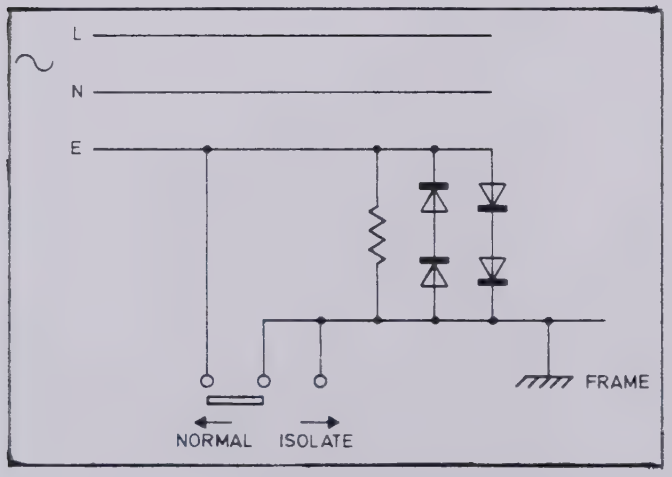


FIGURE 3-3 DIODE ISOLATION NETWORK

Magnetically Induced Interference

If the two input channels are being used in the differential input mode, i.e. with CH1-CH2 displayed, care should be taken to see that the input leads to the two input BNC sockets on the front panel are arranged to be as close together as possible. If a loop of any appreciable area is formed by the two leads there is a possibility of interference being generated within the leads by stray alternating magnetic fields caused either by the instrument itself or by other apparatus. This interference can be significant even with fully screened input leads.

3.9 THE 4103 OUTPUT UNIT OPTION

The 4103 output unit provides the user of the OS4100 with a means of obtaining fast, inexpensive permanent records of displayed traces. It may be used with a wide variety of pen recorders of either XY or strip chart type. Both channels are available simultaneously for recorders with two pens. Alternatively the two channels may be reproduced sequentially on single pen recorders. A synchronized X ramp is available for use with XY recorders. Alternatively the CH1 and CH2 outputs can drive an XY display directly. The internal contacts can be used to control a chart motor and/or pen lift if required.

Chart Recorder Speed

The 4103 offers a wide range of read-out rates to suit the recorder being used. The rate should be chosen by considering the following:

1. A slow read-out rate, while faithfully reproducing the stored signal, will also show the discrete levels in the output waveform. A faster read-out rate and pen recorder speed will tend to smooth the output waveform.
2. If too fast a read-out rate is chosen, the pen recorder may be unable to follow any large amplitude fast change of signal. This is the slew rate limitation of the recorder.

The optimum read-out speed for any particular stored waveform is thus the maximum at which the pen recorder is capable of tracking the signal. The bandwidth of the 4103 output amplifiers is d.c. to 16kHz (−3dB) which is well above the limitations of most pen recorders.

Using with a pen recorder

1. Connect the CH1, CH2 and X-ramp BNC sockets on the read sub-panel as required.

   On single trace operation, the same signal will be present at CH1 and CH2 outputs. Set the sensitivity of the pen recorder inputs to accommodate ±400mV full scale on CH1 and CH2 and 0 to +1V for the X-ramp, i.e. each cm of C.R.T. deflection in X or Y corresponds to 100mV of output level.

   When the 4103 is not reading-out, the analog outputs return to 0V. This corresponds to mid screen on the C.R.T. display for the CH1 and CH2 outputs, and thus the recorder pen(s) should be set to mid scale unless specifically required otherwise. The ramp output moves positive from 0V, however, and the pen should be positioned to allow at least 1V positive travel for this signal.

2. Connect, if required, for remote start/pen lift.

   Note: The relay contacts are unprotected and inductive loads should be suppressed to stay within the contact rating.

3. The delay time from the closure of the relay contacts to the start of read-out is set by a preset control (START UP DELAY) on the rear sub-panel.
4. Obtain the required trace(s) on the OS4100 and store it using the SINGLE SHOT or HOLD functions. If the SPLIT TRACE facility is being used, the trace stored with this control will appear at the CH2 output, the other trace appearing at the CH1 output.
5. Set the required read-out rate on the PLOT SPEED switch on the rear sub-panel. The calibrated times are per cm of unexpanded C.R.T. deflection and should be multiplied by ten to obtain the total read-out time.
6. Set the PLOT MODE switch on the rear sub-panel to the MANUAL START position.
7. Press the PLOT O/P START button on the front panel of the OS4100 to initiate the read-out cycle. Note that the OS4100 is prevented from accepting new data into the store during a read-out cycle and the display will be frozen. The PLOT O/P indicator will light to indicate that a read-out cycle is in progress.

Plot Modes

The PLOT MODE switch on the rear panel selects one of three operating modes:-

MANUAL START:

In this mode a single read-out cycle may be initiated either by pressing the front panel START button or by applying a TTL low level, or contact closure to ground, to the rear panel REMOTE START input. The front panel indicator lamp will light immediately the start command is given and remain on for the duration of the read-out cycle.

AUTO START:

This facility is used in conjunction with the SINGLE SHOT store sequence on the OS4100. Whenever the STORED indicator lamp is lit to indicate the completion of a single shot store sequence, a single read-out cycle will be initiated. At the end of this read-out cycle the timebase of the OS4100 will be armed automatically, ready to execute a further single shot store sequence upon receipt of a trigger signal. In this manner the instrument may be left unattended to monitor and record intermittent transient signals.

Note that to initiate the procedure it is first necessary to press the ARM button to start the single shot store sequence.

Note also that a read-out cycle may still be started in response to the START button or a REMOTE START input command as for the MANUAL START mode. At the end of a read-out cycle started in this way, the timebase will be re-armed.

CONTINUOUS:

With the PLOT MODE switch in this position, a read-out cycle may be initiated in the same manner as the MANUAL START mode. However, instead of just a single sweep being generated, the unit will now read-out continuously until the START button is pressed again (or a REMOTE START command given). The indicator lamp associated with the START button on the front panel will be lit while the output unit is reading out.

Plot Market Output

If the CONTACTS output is used to start up a chart recorder motor, the START UP DELAY control would normally be set to allow the recorder to accelerate to full speed before information appeared at the CH1 and CH2 output socket. It if is required to mark the exact start of the recorder information, with an event marker pen say, the PLOT MARKER output should be used. This provides a TTL logic level signal which goes 'high' at the start of the recorded information and 'low' immediately at the end of it. The loading on this output should not exceed that permitted for a standard low power Schottky gate.

Function Generation

Although primarily intended to be used to drive pen recorders, the analog outputs can be used for other applications.

In the continuous mode the 4103 acts as a function generator, continuously repeating the one or two waveforms stored. Thus a single transient can be recorded at one speed and re-generated continuously at another faster or slower speed within the available stepped range of PLOT SPEED (20sec/cm to 5ms/cm). As the sample density is 100 samples/cm (50 samples/cm for dual trace or split trace) the range of output sample rates available is 20kHz to 5Hz (10kHz to 2.5Hz for dual or split trace).

Functions may be written manually on the screen of the OS4100 by use of the shift control or an externally controlled input during a very slow recording scan. A single scan may be started by use of the MANual TRIGger button and a second trace may be written by using the SPLIT TRACE facility. The two patterns would then be generated simultaneously from the CH1 and CH2 outputs.

3.10 ADDITIONAL FACILITIES

CAL

The calibrated output pin provides a d.c. coupled positive-going square wave of 1 volt ± 1% peak amplitude and 1kHz ± 1% frequency for calibration and probe compensation checks. Shorting the CAL pin to the ground terminal below it, will produce a square current waveform of 1mA in the shorting link. This can be used for current probe calibration.

Use of Passive Probe

The two type PB12A passive probes supplied with the instrument may be used either as direct X1 probes or as X10 divider probes, selected by means of the slide switch located in the body of the probe itself. When used in the X1 mode, the input capacitance at the probe tip will be equal to the 28pF input capacitance of the instrument itself plus the effective capacitance of the probe lead (approx. 60pF total). This may load the signal source in some applications and it is thus advisable to use the

4.1 SYSTEM DESCRIPTION

A more detailed understanding of the functions of the instrument may be obtained by studying the block diagram (Fig. 4-1). Signals applied to the CH1 and CH2 input sockets are handled by two identical pre-amplifier and attenuator circuits. These provide amplified signal outputs to two voltage-to-time converters in addition to a trigger pick-off signal which may be selected by the trigger source switch. The front panel controls associated with the pre-amplifiers are the VOLTS/cm switch, variable gain, Y shift and balance, together with the X10, invert, low pass filter, and sum buttons. The voltage-to-time converters produce a train of output pulses at a repetition rate of 1MHz and a pulse width proportional to the instantaneous amplitude of the signal received from the pre-amplifier. These variable width pulses are used to gate a high speed binary counter thus producing an 8 bit binary encoded representation of the signal level at 1μs intervals. When the instrument is operated in the single trace mode only the output of the appropriate voltage to time converter is used; in the dual trace mode the counter is gated alternately by the two converters and thus the 8 bit data stream from the counter represents alternately CH1 and CH2 input signals.

Each group, or byte, of 8 bit data produced by the counter represents the instantaneous signal amplitude at a particular time. Since an 8 bit binary number represents 256 (=2^8) unique levels the signal amplitude is quantized to the nearest $\frac{1}{256}$ (=0.4%). As the total displayed vertical range on the C.R.T. is 8.5cm this represents a vertical resolution of 0.33mm or 30 steps per cm.

The horizontal resolution of the display is a function of the store size and the maximum conversion rate of the analog-to-digital converter. The OS4100 is fitted with an 8 bit x 1024 main store and has a displayed trace length of 10.2cm thus providing a horizontal resolution of 0.1mm or 100 samples per cm.

Since the maximum A/D conversion rate is 1MHz the maximum equivalent timebase sweep speed available is 100μs/cm. Note that these figures apply only when the expansion control is in the X1 position. When the full X10 expansion is in use, the horizontal sample density is 10 samples per cm and maximum sweep speed is 10μs/cm. Note also that when the instrument is being used in the dual trace mode the horizontal sample density of each trace will be only half that given above for the single trace mode.

The sampling rate used is controlled by the TIME/cm switch. The rate used on any given range is shown in Table 1. Note that the analog to digital converter system always runs at its maximum rate of 1MHz and the actual sampling rate is determined by the rate at which samples are loaded into the two stores.

Data from the analog to digital converter is entered into the delay store. This store functions as a 256 bit long shift register so that data bytes entered into the input appear at the output 256 samples later. This shift register performs a function similar to the analog delay line found in conventional oscilloscopes in providing the capability of viewing the input signal prior to the trigger point. Since the sample rate of the delay store is always equal to the sample rate of the main store, the amount of delay provided is a constant 256 sample points equal to 2.56cm of the display regardless of the timebase range.

The data entered into the main store may be either direct from the analog-to-digital converter (signal delay off) or via the delay store (signal delay on). The entry of data is supervised by the control logic, which also provides timing signals to the high speed counter. The control logic receives a trigger pulse from the trigger amplifier and this initiates a data entry cycle. During this data entry cycle the control logic supplies a sequentially stepped 10 bit write address to the store so that the data bytes are loaded into the correct store locations.

Quite independently of any data entry or writing operation occurring, data is continuously read out of the store into one or both of the digital-to-analog converters. When the instrument is used in the T-Y mode the signal data is supplied to the 8 bit Y channel digital-to-analog converter and a 10 bit digital ramp is supplied to the X channel digital-to-analog converter to provide a 1024 step staircase ramp for the horizontal sweep on the C.R.T. display. In the X-Y display mode alternate samples corresponding to CH2 signal data only are supplied to the 8 bit Y channel digital-to-analog converter, with the remaining samples, corresponding to CH1 signal data, fed to the X channel digital-to-analog converter. Note that in this case the X channel digital-to-analog converter is used as an 8 bit converter only.

The outputs of the two digital-to-analog converters are supplied to the C.R.T. deflection plates via high voltage output amplifiers. Since the rate at which data is read from the store is determined only by flicker considerations, the output amplifiers need only be simple low bandwidth circuits. Dot joining may be performed if required at this stage by introducing identical low pass filters into both X and Y channels.

The data outputs of the store are also supplied to the 4103 output unit when fitted. This unit may read data from the store in a manner similar to the C.R.T. display drive circuitry, but at a rate under control by the PLOT SPEED switch on the output unit.

4.2 Y ATTENUATOR AND PRE-AMPLIFIER

The CH1 and CH2 amplifiers have identical circuits. Consequently, only CH1 will be described, with reference to Fig. 6-1.

The input signal is introduced, via the front panel socket, SKA, to the coupling switches, S11–S13.

The signal may be A.C. coupled by C10 when S11 is depressed, or D.C. coupled when S13 is depressed. Operating S12 disconnects the input signal and grounds the input of the amplifier for reference.

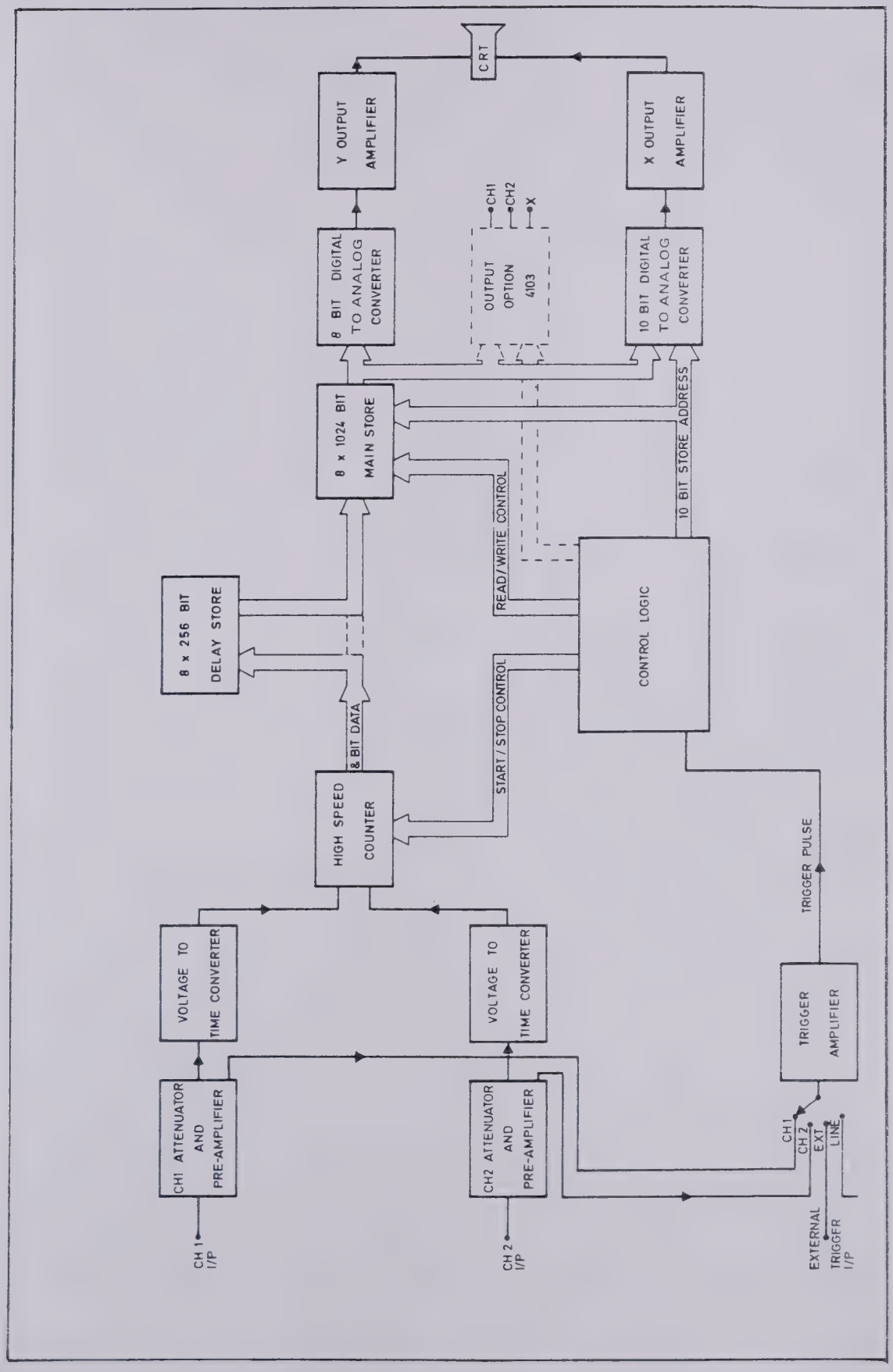


FIGURE 4-1 BLOCK DIAGRAM

Input sensitivity selection is performed by S10. S10(a) produces passive attenuation of the signal to the first amplifier, IC100. There is no attenuation for ranges 1–50mV/cm, ÷10 for 0.1, 0.2 and 0.5V/cm and ÷100 for 1, 2 and 5V/cm. C106 and C101 set the h.f. response on the ÷10 and ÷100 stages respectively, and for each division ratio there is a trimmer to standardize the input capacitance. C112 (÷1), C108 (÷10) and C103 (÷100).

R105 sets the input resistance of the amplifier at 1MΩ, while R109 and diodes, D100 and D101, serve to limit the input voltage to IC100 to ±5V and protect against applied inputs of up to 400V peak.

IC100 is configured as a non-inverting amplifier, whose gain is controlled by resistor network, RN10 and S10. The input offset voltage of IC100 is nulled by front panel preset, R101 (fine), and internal preset, R112 (coarse). The gain of this stage is set at x20 for the 1, 2 and 5mV ranges and at x2 for all the lower sensitivity ranges. The gain is increased by a factor of 10 by operating S102, thereby providing the 100, 200 and 500μV/cm sensitivities.

The final section of the sensitivity selection is performed by the passive attenuation of the output from IC100 in the following manner: on the 1mV range ÷1, on the 2mV range ÷2 and on the 5mV range ÷5, this sequence repeating four times with reducing sensitivity. By the means outlined above, the sensitivity at the input to IC101 is maintained at a constant 20mV/cm.

R119 and C118 provide a 10kHz low pass filter at the input of IC101 when selected by S103. IC103 is configured as a fixed gain, non-inverting, amplifier.

The input offset voltage is nulled by preset, R122. TR10 and its associated components provide h.f. neutralisation of the signal fed back to the input of IC100 via stray capacitance. The gain of the neutralization amplifier is adjusted by R16.

The operation of IC102 can best be described with reference to Fig. 4-2. When neither INVert or ADD functions are selected, inputs B and C are grounded and the signal from IC101 is introduced via input A. IC102 then functions as an inverting amplifier with gain set by R135. When INVert is selected, input A is grounded and the signal enters via C. The amplifier is then non-inverting with gain set by R143. If ADD is selected, the CH2 signal from IC201 output is added via input B, with the gain adjusted by R126. Y shift is accomplished by the current Is added at pin 2, produced by TR100, front panel shift control, R100, and the associated components. As the shift current is unipolar, R130 produces an offset to null Is when the shift control is centred.
The VARiable gain control, R10, produces a variable attenuation to allow interpolation between switched ranges. Note that the cross-channel signal to the CH2 ADD input is taken off before R10.

The components, D104, D105, D106, limit the output from IC102 when the latter is overdriven. TR101 then buffers the signal before it enters the A to D converter.

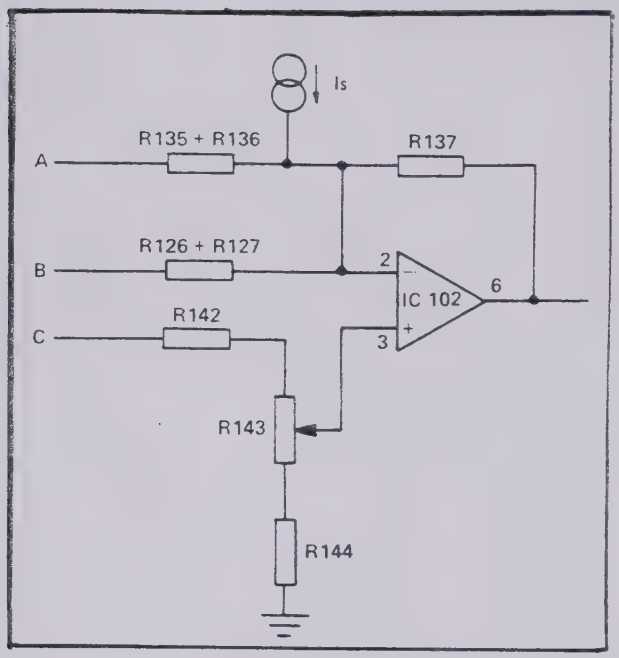


FIG. 4-2 Y AMPLIFIER: IC102 IN TEXT

4.3 ANALOG TO DIGITAL CONVERTER

4.3.1 CONVERSION TECHNIQUE

The conversion of analog input signals to digital data is performed with a single ramp counting method. Referring to Fig. 4-3, the input signal is applied to a comparator, together with a linear ramp signal as shown. At the start of the ramp clock pulses are applied to a binary counter. When the voltage level of the ramp is equal to the input signal level the count-enable signal goes low ans the binary counter stops counting. Clearly the number of clock pulses supplied to the counter in this period is proportional to the input signal level and at the end of each conversion cycle the contents of the binary counter are latched into the output data register and the counter is reset to zero, as is the linear ramp generator.

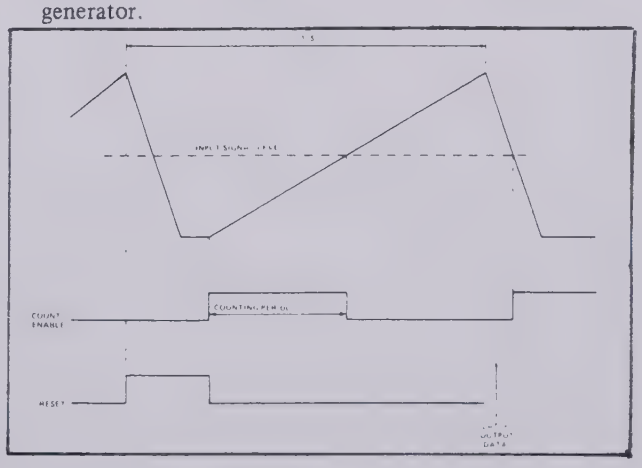


FIG. 4-3 RAMP CONVERSION TECHNIQUE

The system is shown in detail in the block diagram, Fig. 4-4. Analog signals from the two pre-amplifiers are applied to independent comparators, one of which is selected as the active device by a control signal, BSW, from the control logic. The linear ramp is applied to the reference inputs of both comparators and the output from the comparator in use is transmitted to the high speed binary counter via a differential output buffer.

In order to complete successive conversions at the required rate (1MHz), it is necessary to use a very high clock frequency (160MHz). Thus the first four stages of the eight bit binary counter are implemented with ECL (emitter coupled logic) devices, and the remainder of the counter with conventional TTL (transistor-transistor logic) devices. Since the voltage levels of these two logic families are different (see Table 4-1) a level translator is required.

The 160MHz clock pulses are derived from an LC oscillator, fed via an ECL buffer stage and applied to the binary counter after being gated with the count-enable signal from the voltage comparators. Note that the first two flip-flops in the binary counter are driven with anti-phase clock signals from the ECL buffer so that they count on opposite clock edges. This allows the counter to resolve half clock periods and thus increases the effective speed of counting.

The high frequency clock pulses are also applied to a ÷16 ECL divider and a ÷10 TTL divider to produce the 1MHz square clock (RAS) which synchronizes the store and control logic operation. This 1MHz clock initiates a reset pulse which:

1. Clears the high speed data counter to zero.
2. Resets the linear ramp generator.
3. Resets the over and underrange detector circuits.

The under and overrange detectors override the data latch to provide zero and full scale outputs respectively if the input voltage applied to the comparators is outside the normal working range. This provides the converter with clean limiting characteristics at the top and bottom of the screen.

4.3.2 CIRCUIT DESCRIPTION

The analog to digital converter components are located on two separate PCB assemblies. The linear section, the voltage comparators and the ramp generator circuit, is on the Y amplifier PCB assembly (circuit diagram Fig. 6-1) and the data counter, clock divider and other digital circuitry form part of the store PCB assembly (circuit diagram Fig. 6-2).

Referring to Fig. 6-1, the analog input signals for CH1 and CH2 are picked off at the emitters of TR101 and TR201 respectively and applied to the two voltage comparators in IC104. A linear ramp signal is generated by the constant current source, TR103, charging the timing capacitor, C135, and buffered by the emitter follower, TR105. One of the two comparators in IC104 is selected to be active by the channel select switches, S104 and

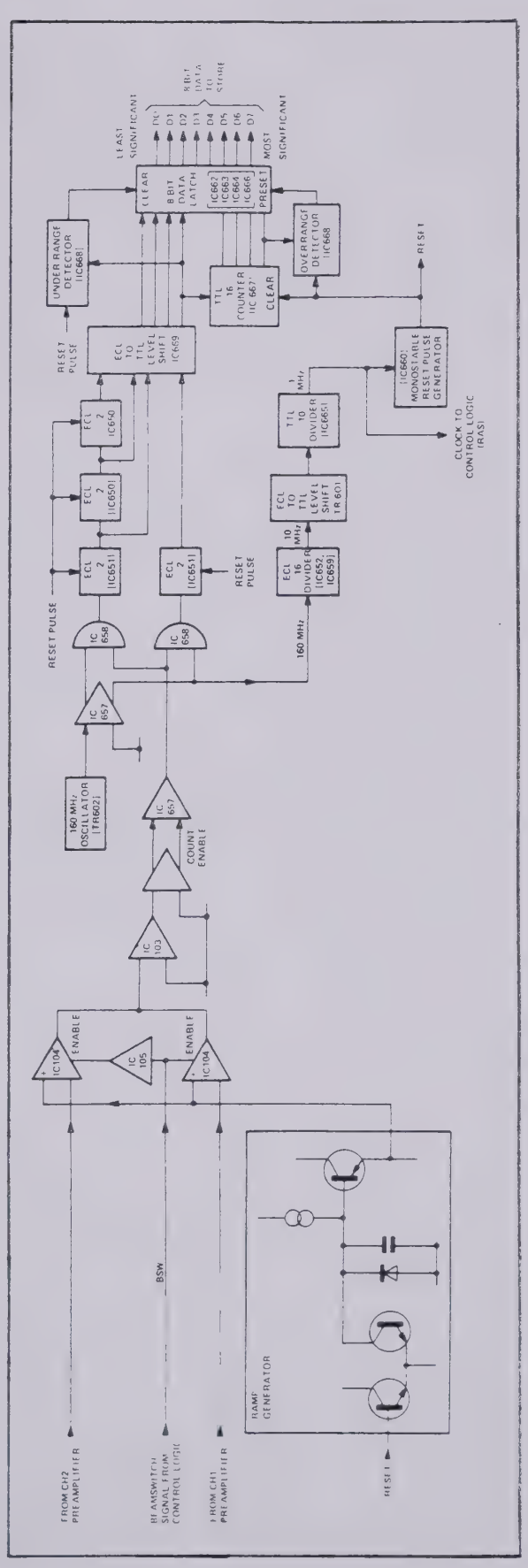


FIGURE 4-4 A/D BLOCK DIAGRAM

S204, and the BSW signal from the store PCB. The level shift network, R169, C138, R168, converts the output of the selected comparator from TTL to ECL logic levels and the line driver, IC103, provides a balanced ECL output for transmission to the counting logic on the Store PCB. The RST (reset) signal from the store PCB goes to a ECL low level for ~60ns at the end of each conversion period and diverts the current from TR107 to TR106 which rapidly discharges the timing capacitor, C135, to the point where the clamp diode, D109, turns on.

Referring to the store PCB circuit diagram, Fig. 6-2, transistor, TR602, forms a stable 160MHz oscillator with its frequency determined by L603/C626, C627. The output is taken via C629 to the differential buffer, IC657B, which produces antiphase outputs at pins 6 and 7. The count-enable signal from the comparators on the Y amplifier PCB is transferred via the buffer, IC657C, to the set/reset flip-flops formed by the four gates of IC658. These two flip-flops provide a gated stream of clock pulses to the first two counter bistables in IC651. Note that both bistables are clocked in parallel, but by antiphase clock signals. The purpose of this is to obtain a greater effective counting speed as shown in Fig. 4-5. By latching the output of the first bistable into a second bistable on the reverse edge of the clock, a resolution of one half of one clock period may be obtained, corresponding to 3ns resolution with a 160MHz clock. The output code for the least significant bit must be gated with the next most significant bit in an exclusive OR gate to obtain a binary counting sequence. Referring to the circuit diagram, Fig. 6-2, this is done after the data output latch in IC661B.

The output of IC651 (pin 14) is applied to a further pair of ECL bistables, IC650, connected as conventional ripple through binary counters. The outputs of all four ECL counting stages are fed to a quad ECL-to-TTL level translator, IC669. The most significant TTL output is taken from IC669, pin 12, via gate, IC666B, and the inverter, IC663E, to a 4 bit counter, IC667, which provides the most significant four bits of the data output. The four least significant bits of the output data are transferred from IC669, via the gates IC666A–D to the output latch IC662 at the end of each cycle. Similarly, the four most significant bits of the output data are transferred from the TTL counter, IC667, via the inverters, IC663A, B, C and F, to a second output latch, IC664. Note that both groups of data bits are inverted before being latched, since the analog signal applied to the comparators on the Y amplifier PCB is inverted with respect to the input signal to the instrument.

The gates, IC666A–D, together with the bistable, IC668B, form the underrange detector. At the start of each conversion cycle the reset pulse is applied to clear input of IC668B, thus setting the Q (pin 9) into a low state and disabling the gates IC666A–D. After 16 counts of the conversion period have elapsed the most significant output of the ECL counting stages at IC669, pin 12, will make a negative transition thus clocking IC668B into the set condition and enabling the gates IC666A–D.

IC668A acts as an overrange detector. If the counter is allowed to count past full scale it will go back to zero and begin to count up again. In doing so the most significant data bit from IC667, pin 8, will make a negative transition and clock IC668A into the set state. This will cause the $\bar{Q}$ output (pin 6) to go low and hold down the clear inputs to the data output latches at pin 1 of IC662 and IC664. Note that due to the signal inversion mentioned above a full scale count corresponds to a data output of all zeros.

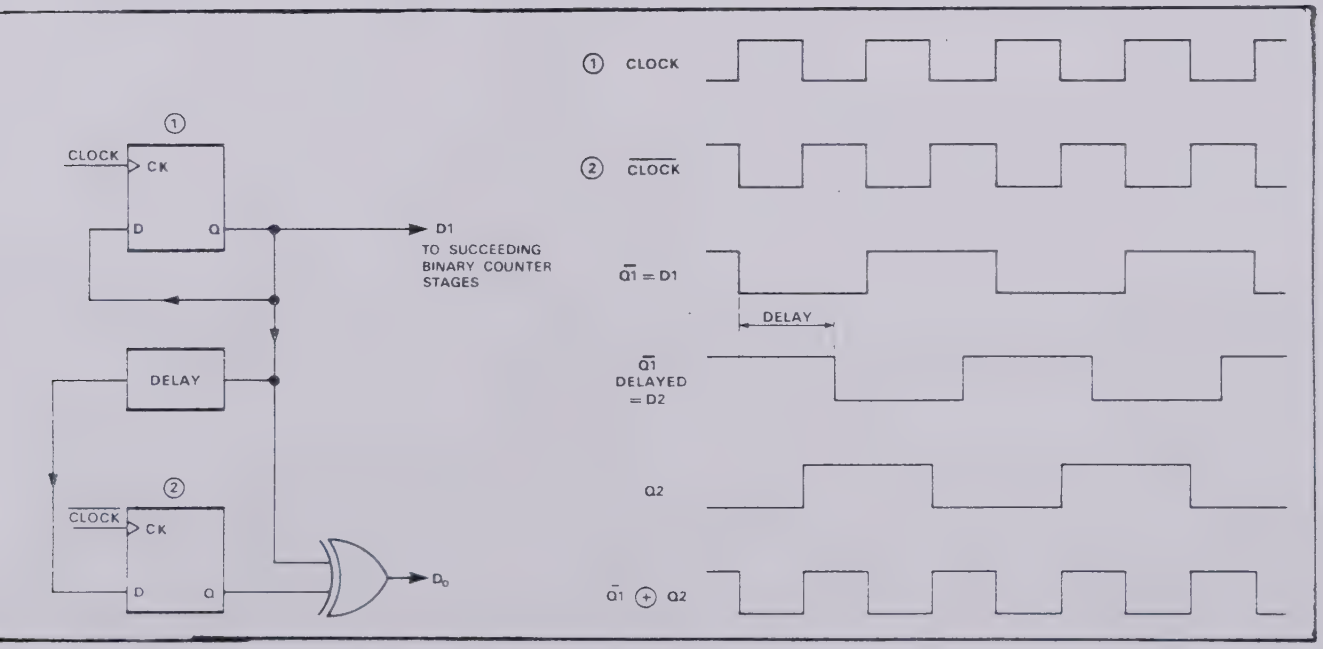


FIGURE 4-5 DUAL PHASE COUNTING TECHNIQUE

An additional divider chain is employed to generate the timing control signals. The 160MHz clock from IC657B, pin 7, is applied to a four stage divider consisting of the two dual ECL bistables, IC659 and IC652. The resulting 10MHz output from IC652, pin 15, is level shifted to TTL levels by the common base transistor stage, TR601. The output of this stage is applied to the TTL decade divider, IC665, to produce the basic 1MHz square wave clock signal for the whole instrument which is known as RAS. IC665 actually contains independent ÷2 and ÷5 stages and the 10MHz signal from TR601 is applied first to the ÷5 stage at pin 11, thus generating a 2MHz intermediate signal at pin 8 which is then divided by 2. This 2MHz intermediate clock signal is employed in the store control logic in order to generate special functions (see section 4.4.5 and 4.4.7). The 1MHz output from pin 9 is used to trigger a one shot monostable, IC660, to provide the reset pulse. This reset pulse is used at TTL levels to reset the most significant 4 bit data counter, IC667, and also to reset the under and overrange bistables, IC668A and B, via the inverter, IC663D. It is also level shifted to ECL levels via the network, R623, C630, R622, and the ECL buffer, IC657A, and used to reset the data counters, IC650, IC651, and sent to Y amplifier PCB to reset the ramp generator.

TABLE 4-1 ECL & TTL LOGIC LEVELS

LOGIC TYPE	LOGIC LOW	LOGIC HIGH
TTL	<0.8V	>2.4V
ECL	>−1.65V	<−0.96V

4.4 STORE AND CONTROL LOGIC

4.4.1 GENERAL DESCRIPTION

A block diagram of the store and control logic is shown in Fig. 4-6. Data from the output latch of the A/D converter is applied to the delay store and the data selector. The delay store, together with its 8 bit address counter, functions as an 8 bit wide, 256 bit long, shift register, clocked at the sampling rate. Data applied to its input will appear at the output 256 sample periods later and it functions as a 'pipeline' store so that pre-trigger information may be viewed. The data selector passes either delayed data from the store or direct data from the A/D converter and is controlled by the SIGNAL DELAY pushbutton on the front panel.

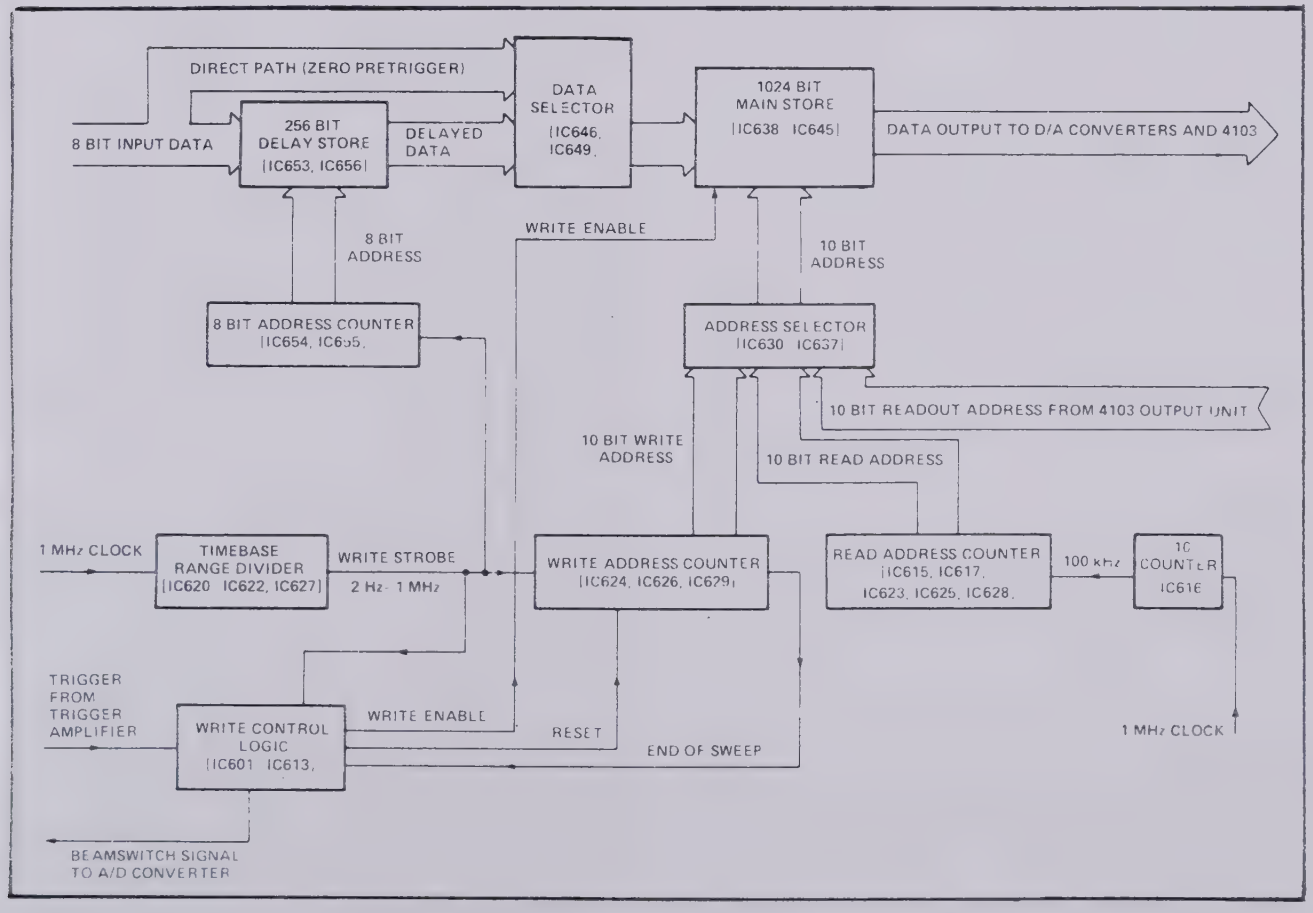

DIRECT PATH (ZERO PRETRIGGER)
8 BIT INPUT DATA
256 BIT DELAY STORE (IC653, IC656)
DELAYED DATA
DATA SELECTOR (IC646, IC649)
1024 BIT MAIN STORE (IC638 IC645)
DATA OUTPUT TO D/A CONVERTERS AND 4103
8 BIT ADDRESS
WRITE ENABLE
10 BIT ADDRESS
8 BIT ADDRESS COUNTER (IC654, IC655)
ADDRESS SELECTOR (IC630 IC637)
10 BIT READOUT ADDRESS FROM 4103 OUTPUT UNIT
10 BIT WRITE ADDRESS
10 BIT READ ADDRESS
1 MHz CLOCK
TIMEBASE RANGE DIVIDER (IC620 IC622, IC627)
WRITE STROBE
2 Hz - 1 MHz
WRITE ADDRESS COUNTER (IC624, IC626, IC629)
READ ADDRESS COUNTER (IC615, IC617, IC623, IC625, IC628)
100 kHz
10 COUNTER IC61E
TRIGGER FROM TRIGGER AMPLIFIER
WRITE CONTROL LOGIC (IC601 IC613)
WRITE ENABLE
RESET
END OF SWEEP
1 MHz CLOCK
BEAMSWITCH SIGNAL TO A/D CONVERTER

FIGURE 4-6 STORE AND CONTROL LOGIC BLOCK DIAGRAM

The signal data from the data selector is applied to the main store which has 1024 locations capable of storing one 8 bit data byte. Which of these 1024 locations is used is specified by the 10 bit (2^{10} = 1024) address input and data may be read from or written into a particular location as determined by the write enable input. Since the store employs random access memory devices, locations may be specified in any order. The address selector may obtain a memory address from one of three sources, viz:-

1. The write address counter. This counter specifies the address of the location into which input data is to be written.
2. The read address counter. This counter specifies the address of the location from which data is to be read for the CRT display.
3. An externally supplied address, normally from the 4103 output option. This specifies the address of the location from which data is to be read for the 4103 analog output unit.

Note that each of these three address sources are quite independent of each other. Normally only the read and write addresses are used and these are selected by the RAS clock signal as shown in Fig. 4-7. When the 4103 output option is fitted and a plot readout cycle is being performed, the readout address is supplied in place of the write address and for this reason data cannot be entered into the store while such a readout cycle is in progress.

The write address counter is under the control of the write control logic and the timebase range divider. A normal data entry cycle is initiated by a trigger pulse from the trigger amplifier. If this is recognized as a valid trigger signal by the write control logic, the reset signal is removed and the write counter is stepped on by the write strobe pulses from the timebase range divider. Each time a write strobe pulse occurs, the write control logic pulses the write enable line to allow one new data sample to be written into the main store at the location indicated by the write address counter. This continues until all 1024 locations of the store have been refreshed with new data and then an end of sweep signal from the write address counter causes the write control logic to reset the counter and disable the write enable line.

Note that the rate at which new data is entered into the store and hence the time taken to complete a recording sweep is determined by the frequency of the write strobe pulses. Since 100 samples represent 1cm of display (at the x1 expansion setting) the period between pulses is $\frac{1}{100}$ x TIME/cm setting.

In the dual trace mode alternate locations in the store are allocated to the two input channels, thus the sampling rate *per channel* is halved. However, since a write strobe pulse must be generated to record data from either channel, the overall sampling rate remains the same for either single or dual trace operation. In dual trace operation it is desirable for the two input channels to be sampled as near simultaneously as possible and thus the write strobe pulses occur in double width 'pairs' as shown in Fig. 4-8. Note that in the single trace condition, Fig. 4-8a, a single data sample is recorded during each strobe pulse and the write address counter is incremented by one count. In the dual trace mode, Fig. 4-8b, two data samples are recorded consecutively and the write address counter is incremented twice during each write strobe pulse. Also shown is the beam-switch signal which is generated by the write control logic to indicate which channel is to be selected at the A/D converter input.

The contents of the store are continually being read out onto the CRT screen irrespective of whether a write cycle is in progress or not. The read address counter cycles through each data location in turn and the corresponding output from the store is loaded into a latch on the Display

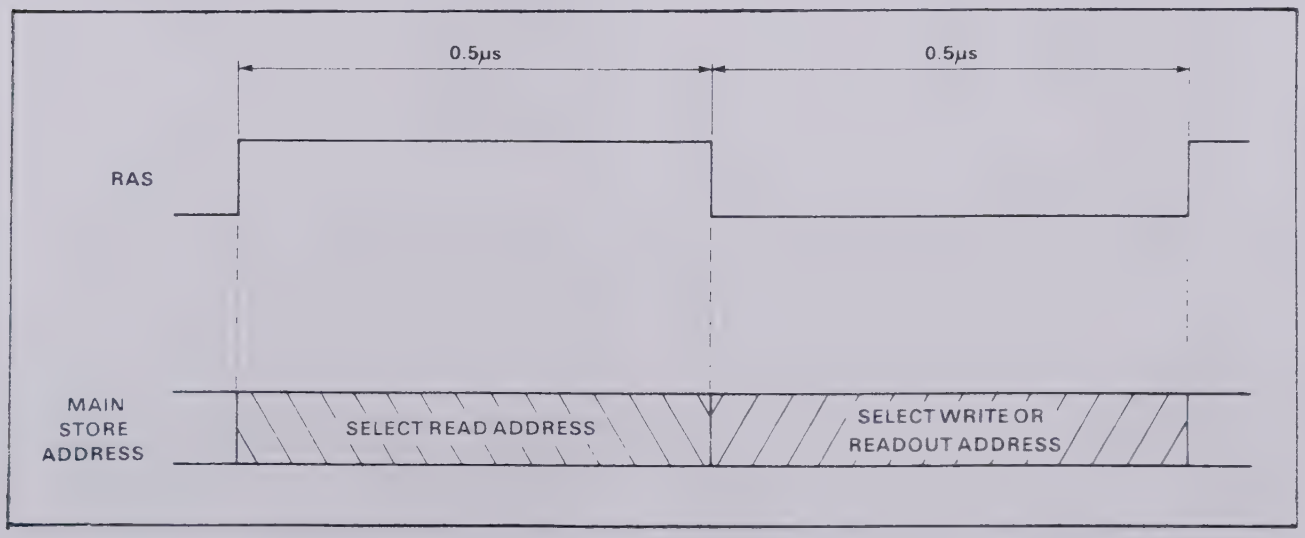


FIGURE 4-7 STORE ADDRESS SELECTION

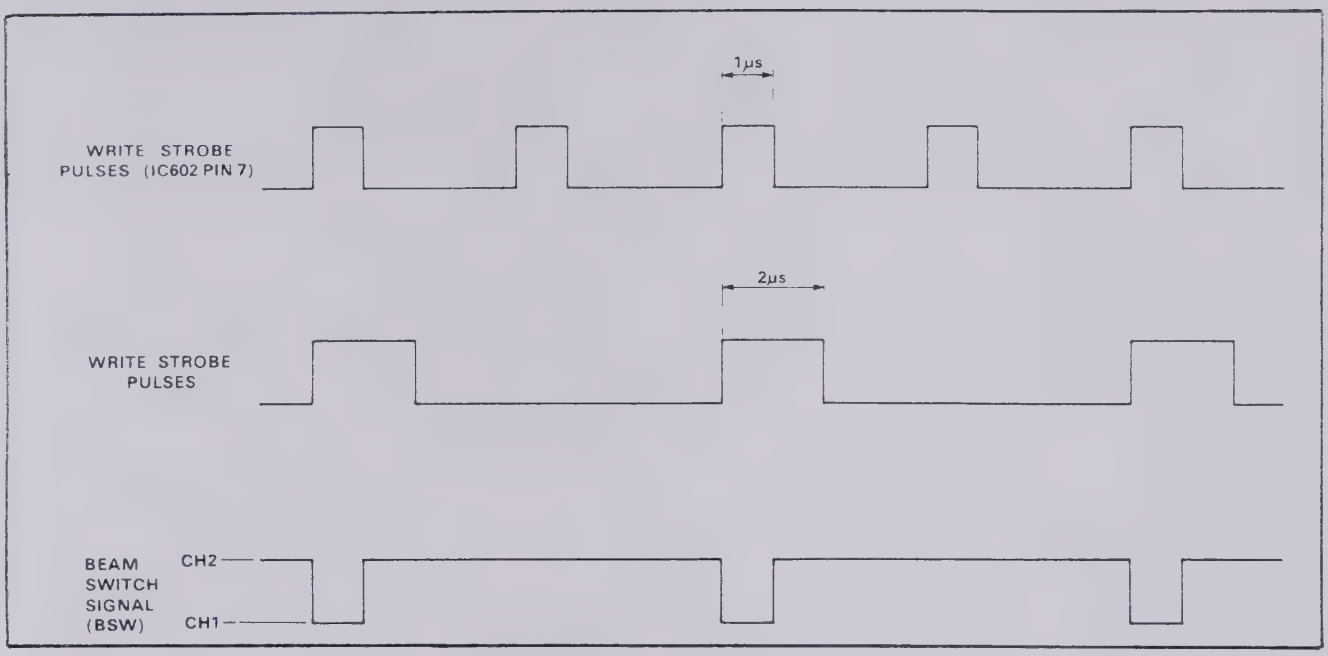


FIGURE 4-8 a + b WRITE STROBE PULSES

PCB. The exact manner in which each data word is read depends upon the display modes:

1. Single trace T-Y display mode. In this case the data words are read from the store in order and displayed on the screen from left to right.
2. Dual trace T-Y mode. Since CH1 and CH2 signals are stored in consecutive locations in the store there are effectively two 512 point signals to be read out rather than a single 1024 point signal. As it is necessary to dot join consecutive samples of each individual signal, they are read out effectively in an 'alternate' mode rather than the 'chopped' mode in which they were recorded. Thus the read address counter scans through all 512 CH1 signal points and then all 512 CH2 signal points. Since the overall data rate is kept constant, the read address counter is now incremented in jumps of two locations at a time. Note the dual trace readout mode is also used when the split trace facility is used with a single input channel operating.
3. X-Y display mode. In the X-Y mode the X data is stored in CH1 locations and the Y data in CH1 locations. Since both X and Y data words must be read out to provide a new displayed sample point the read address counter must step through a pair of addresses at each update.

4.4.2 CIRCUIT DESCRIPTION: DELAY AND MAIN STORES

All the store and control logic is located on the store PCB assembly; see Fig. 6-2 for the circuit diagram. Throughout the following descriptions mnemonics are used to indicate various signals. These mnemonics are shown on the circuit diagram and are also listed in section 4.4.8.

All logic timing is referred to the 1MHz RAS square wave provided by the analog to digital converter logic. This signal is available at pin TP2 at the rear top edge of the PCB. The timing of the store functions is shown in Fig. 4-9. New data from the A/D converter is latched into the converter output latches, IC662 and IC664, on the rising edge of RAS. If the write strobe pulse, WSP, at IC602, pin 7, is low during this time then the data is ignored. If WSP is high the data is loaded into the stores in the following sequence.

The 8 bit delay store address counter formed by IC609A, IC654 and IC655 is incremented on the rising edge of RAS. After the delay stores, IC653 and IC656, have settled to the new address, the data appearing at their outputs will be the data that was written in the last time this address was accessed. Since there are 256 locations in the delay store, this information will be 256 samples 'old'. The data selectors, IC646 and IC649, select either the delayed data from the delay stores or the current data from the A/D output latches, IC647 and IC648. The data selectors are controlled by the SIGNAL DELAY pushbutton, S604, via the debounce latch, IC604, and the select inputs of IC646 and IC649, on pin 1. A high level at this point selects delayed data.

At the beginning of the store entry cycle a monostable, IC618B, is triggered by a combination of RAS and WSP via the gate, IC610C. The pulse from IC618B (pin 5) lasts approximately 550ns and the falling edge triggers a second monostable, IC618A. The pulse from IC618A is 300ns long occurring while RAS is low (see Fig. 4-9) and is called the write enable pulse, WEP. This pulse, when applied to the write enable input of either delay or main.

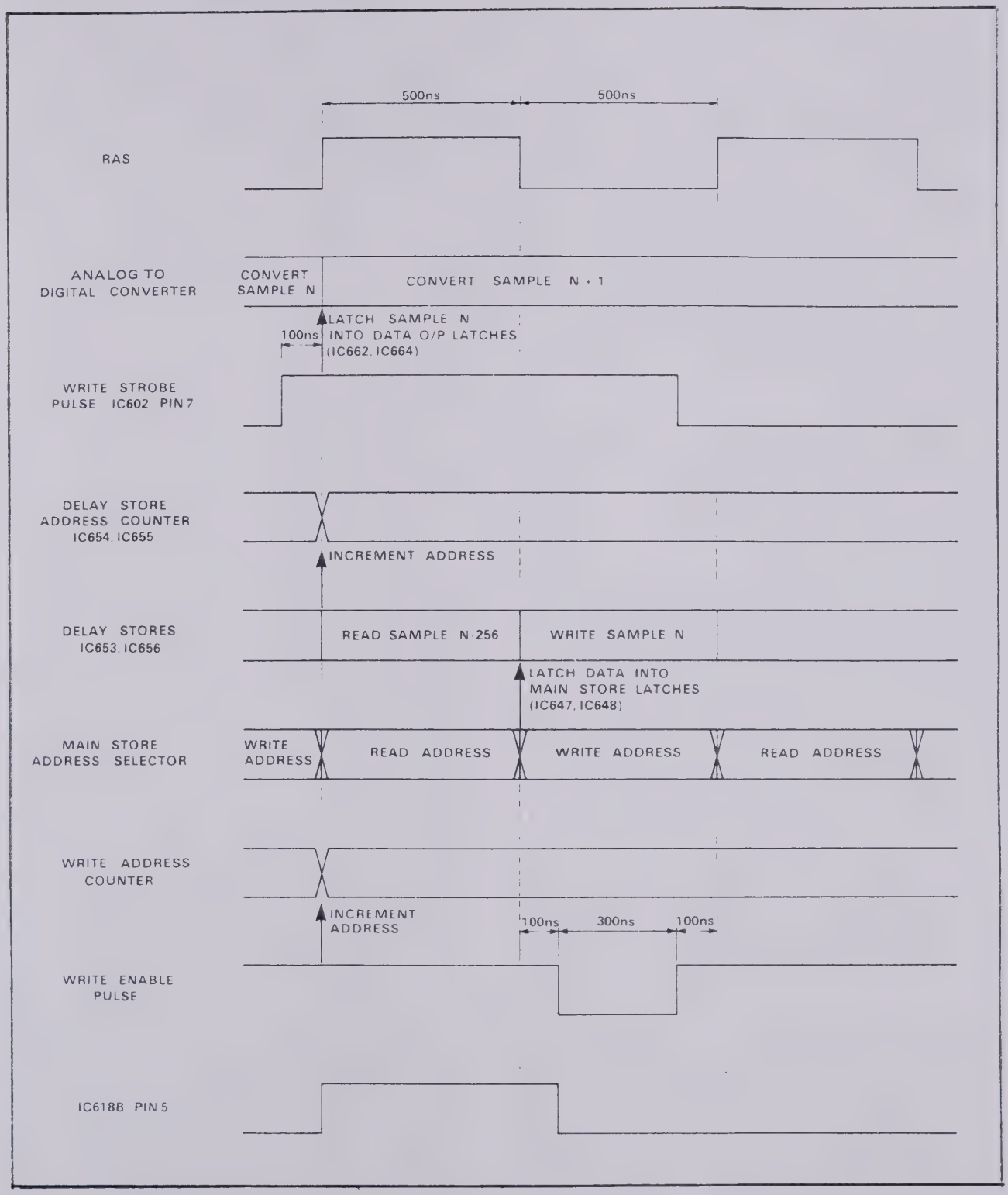


FIGURE 4-9 STORE TIMING

stores, causes the store to write the data present on the inputs into the location specified by the store address inputs. In doing so it automatically erases the data previously held in that location. The WEP command is applied directly to the delay stores from IC618, pin 4, and via IC611A to the main stores, IC638–IC645.

The data inputs of the main stores, IC638–IC645, pin 11, are derived from the main store latches, IC647 and IC648. These are clocked by the falling edge of RAS, and hold the data present at the data selector outputs at this time. The address inputs of the main store, pins 8 to 14 of each device, are obtained via five dual 4 input multiplexers, IC630–IC637. These devices are controlled by the A and B select inputs (pins 14 and 2 respectively) allowing 4 possible address sources. The B select input is $\overline{RAS}$, the main clock signal, and the A select input is $\overline{RDO}$, which goes low when the output option is plotting. The connections to the inputs are omitted from the circuit diagram for the sake of clarity, but are labelled W0 to W9 for the write address, R0 to R9 for the read address and A0 to A9 for the output unit address. Note that two of the four inputs to each address selector are strapped so that when $\overline{RAS}$ is low, the read address is always selected regardless of the state of $\overline{RDO}$. Thus when $\overline{RDO}$ is high, that is when the output unit is inactive, the read address is selected while RAS is high and the write address while RAS is low. If the output unit is plotting then $\overline{RDO}$ goes low, and the read address is still selected while RAS is high but the output unit address is selected while RAS is low. This continuous multiplexing of two addresses allows the store to be written into and read from, effectively at the same time.

4.4.3 WRITE CONTROL LOGIC

Data is normally written into the store following a trigger pulse from the trigger amplifier on the Display PCB. Referring to Fig. 6-2, the incoming trigger pulse, TRG is applied to IC606A and S610, the trigger slope switch, $\overline{TRG}$, or its inverse is applied to IC613B and the rising edge will cause a logic '1' to be clocked through from the D input (pin 12) to the Q output (pin 9), and applied to the D input (pin 2) of IC613A. The clock signal to IC613A is derived from RAS and WSP via IC610C and makes a positive transition whenever a store entry cycle occurs, causing the Q output of IC613A (pin 5) to go high at the beginning of the first store entry cycle after a trigger pulse is received. This allows write enable pulses (WEP) to be supplied to the main stores via IC611A and also removes the reset from the write address counter IC609 (pin 14), IC624, IC626 (pins 12 and 13), and IC629A (pin 15). Data will now be written into the main stores whenever a store entry cycle occurs (as determined by WSP). The write address counter is incremented during each store entry cycle and at the end of the sweep the counter will return to zero. This causes the most significant bit, IC629A (pin 5), to go low thus clocking IC612A into the 'set' state. The $\overline{Q}$ output of IC612A (pin 6) goes low resetting IC613 and thus disabling the WEP signal to the main stores and applying a reset signal to the write counter. If the timebase is functioning in the normal continuously triggered mode, the single shot ($\overline{SSH}$) input to IC606D, pin 13, will be high and a logic low will be applied to the clear input of IC612B (pin 14) causing it to be reset. When this occurs the Q output of IC612B (pin 9) goes low and applies a reset to IC613B at pin 13. The Q output of IC613B (pin 9) goes low in turn and applies a reset to IC612A at pin 15. Since the Q output of IC612A (pin 5) is connected to the preset input of IC612B at pin 10, the Q (pin 9) of IC612B returns high and the bistables are now in their original state awaiting the next trigger input. This sequence of operation is shown in Fig. 4-10A in table form. The states shown separated by dashed lines represent transitional states; the term 'set' applies to a bistable whose Q output is high.

The sequence of operation in the single shot mode is broadly similar, as shown in Fig. 4-10B, except that since the $\overline{SSH}$ line at pin 13 of IC606D is low, the resetting sequence following IC612A being set will not occur instantaneously. Instead the system locks up after a single sweep has finished until IC612B is clocked with a negative transition caused by pressing the ARM button on the front panel. Fig. 4-10B also shows the state of the single shot indicator LED's, D64–D66. These are controlled by IC607 which is a 3 line to 8 line decoder with open collector outputs. This decodes every possible combination of the three input lines A, B and C, together with the enable input G and pulls down one of its eight outputs. Two of the input lines, A and B, are driven from outputs of bistables IC612A and IC613A to monitor the state of the write control bistables. Input C is controlled by the $\overline{SSH}$ line to indicate whether the single shot mode is in use. The enable input, G1, is fed from the output of a monostable pulse generator, IC608, which is clocked by the trigger input to IC613B and delivers a pulse of about 200ms duration whenever the write control logic is triggered. In the normal (repetitive trigger) mode the ARMED and STORED LED's are not used but the TRIGGERED LED is flashed by the pulse from IC608. In the single shot mode the three LED's show the status of the write control bistables as described in Fig. 4-10B. Note that the TRIGGERED LED now stays lit for the duration of the writing sweep.

The monostable, IC608, also serves to detect the presence of continuous trigger pulse for the AUTO TRIGGER facility. If trigger pulses at a rate greater than approximately 5Hz are present, the $\overline{Q}$ output at IC608, pin 6, will be permanently low. When trigger signals cease, however, the output will go high and if the ATO line is also high (indicating that the AUTO TRIGGER button on the Display PCB is pressed) the output of gate IC603 (pin 3) will go low. This causes a high at IC603, pin 8, and a low at IC603, pin 11, which is applied to the preset input of IC613A at pin 4, thus causing the main store to write continuously. Note that the $\overline{SSH}$ line is applied to IC603D, pin 13, so that the AUTO TRIGGER is automatically disabled when using the single shot mode.

STATE	IC613B	IC613A	IC612A	IC612B
Awaiting Trigger (from TRG)	Reset	Reset	Reset	Set
Triggered: Awaiting next store entry cycle to begin	Set (By trigger pulse)	Reset	Reset	Set
Writing into main store	Set	Set	Reset	Set
End of write sweep: MSB of write counter goes low (MSB is IC629A pin 5)	Set	Set	Set (By negative edge of MSB)	Set
	Set	Reset by low on IC612A $\overline{Q}$ (pin 6)	Set	Reset by low on IC612A $\overline{Q}$ (pin 6)
	Reset by low on IC612B Q (pin 9)	Reset	Set	Reset
	Reset	Reset	Reset by low on IC613B Q (pin9)	Reset
	Reset	Reset	Reset	Set by low on IC612A Q (pin 5)
Awaiting next trigger	Reset	Reset	Reset	

FIGURE 4-10A WRITE CONTROL BISTABLE SEQUENCE: NORMAL MODE

STATE	IC613B	IC613A	IC612A	IC612B	LED's
Awaiting Trigger (from TRG)	Reset	Reset	Reset	Set	Armed
Triggered: Awaiting next store entry cycle to begin	Set (by trigger pulse)	Reset	Reset	Set	Triggered
Writing into main store	Set	Set	Reset	Set	Triggered
End of write sweep: MSB of write counter goes low (MSB is IC629A pin 5)	Set	Set	Set By negative edge of MSB	Set	Stored
Awaiting ARM signal from front panel	Set	Reset by low on IC612A Q (pin 6)	Set	Set	Stored
ARM button pushed	Set	Reset	Set	Reset: clocked by ARM button	Stored
	Reset by low on IC612B Q (pin 9)	Reset	Set	Reset	Stored
	Reset	Reset	Reset by low on IC613B (pin 9)	Reset	Armed
Awaiting next Trigger	Reset	Reset	Reset	Set by low on IC612A Q (pin 5)	Armed

FIGURE 4-10B WRITE CONTROL BISTABLE SEQUENCE: SINGLE SHOT MODE

4.4.4 WRITE ADDRESS COUNTERS

There are two write address counters in the store control circuitry: the delay store address counters comprising IC609A, IC654 and IC655, and the main store write address counter comprising IC609, IC624, IC626 and IC629A. The delay store counter is 8 bits long and runs continuously regardless of trigger status or front panel controls. The main store counter is 10 bits long and runs only when data is to be recorded in the main (displayed) store.

The write address counter for the delay store is an 8 bit ripple through counter comprised of the bistable IC609A together with the two 4 bit counter packages IC654 and IC655. The address output is labelled S0 to S9, with S7 being the most significant bit. Note that only three of the 4 bistables available in IC655 are used. The timing of the counter is shown in Fig. 4-11. The first bistable (IC609A) is a J-K type, with RAS applied to the clock input and WSP, the write strobe pulse, from the timebase range divider section applied to both J and K inputs. The counter is incremented whenever a negative transition of $\overline{RAS}$ occurs while WSP is high. In the single trace mode WSP is a 1μs long pulse occurring at intervals determined by the sample rate (see Table 3-1). In the dual trace mode a double length WSP signal is generated so that CH1 and CH2 signals may be recorded almost simultaneously. A feedback loop in the range divider circuitry ensures that CH1 is recorded first, during which time the least significant bit of the address, SO, is low. This address line is also used as the beamswitch control signal, BSW, which selects the required input channel to the ADC. Note that because of the 1μs time delay incurred in the analog to digital conversion, the sense of the BSW signal is reversed with respect to SO: BSW high indicates that CH1 is to be converted whereas the CH1 information is written into a store location with SO in the low state. Reference to Fig. 4-9 should make this clear.

The main store write address counter is a 10 bit ripple through binary counter comprising either IC609A or IC609B, together with the two 4 bit counter packages, IC624 and IC626, and the bistable, IC629A. IC601 is a quad two input data selector and selects either IC609A or IC609B as the first stage of the write address counter, dependent upon the state of the select input, pin 1.

In the single trace mode the select input of IC601 is at a high level, and the B inputs are fed through to the corresponding outputs. Thus the Q output of IC609B (pin 9) is connected to the least significant write address line, WO, and also the clock input of the following stage of the write address counter. The reset inputs of all stages of the counter are controlled by IC613A so that counting commences from zero when IC613A is set. Note that the two individual bistables in the counter, IC609B and IC629A require negative logic reset (or clear) inputs and are connected to the Q output of IC613 (pin 5), while the 4 bit counter packages, IC624 and IC626, require positive logic clear inputs and are thus connected to the $\overline{Q}$ output of IC613 (pin 6).

The timing of the counting sequence is identical to that shown for the delay store address counter in Fig. 4-11A. The clock input of IC609B (pin 13) is driven by $\overline{RAS}$ and the J and K inputs (pins 11 and 12 respectively) by WSP, thus whenever WSP is high during a negative transition of $\overline{RAS}$, IC609B will toggle and the write address will be incremented.

An additional constraint is placed upon the main store write address counter during dual trace operation. Since CH1 and CH2 data is alternately written into even and odd numbered store locations respectively, and since this data may originate from the delay store (if the signal delay is in use) it is necessary to synchronize the two store address counters to the extent that the respective least significant address lines, SO and WO, are locked together. This is achieved by using the least significant address line of the delay store address, So, from IC609A, as the least significant address line, WO, of the main store write address. Thus, during dual trace operation the select input (pin 1) of IC601 goes low and the A inputs of the data selector are transferred to their respective outputs. The Q output (pin 5) of IC609A is then connected to the WO address line and the clock input of the following stages of the write address counter. Note that while the most significant 9 bistables in the write address counter chain are reset by IC613A as in single trace operation, the least significant bit will now be continuously changing. This implies that location 1 may or may not be written into the start of a write sweep. However, the first four locations of the store are not displayed since flyback blanking is in operation while these are being read out.

4.4.5 TIMEBASE RANGE DIVIDER

The timebase range divider circuitry can be split into two functions:

1. The frequency divider chain comprising IC620, IC621, IC622, IC627A.
2. The retiming circuitry comprising IC601, IC602, IC610B, IC611B.

The frequency divider chain produces a pulse with a repetition frequency dependent on the setting of the TIME/CM switch, S61. The relationship between this repetition frequency and the timebase range setting is simply determined by the number of samples stored per centimeter of trace, i.e. 100 in the single trace mode and 50 in the dual or split trace modes. Table 4-2 shows the frequency selected for each timebase range. These frequencies are derived from the basic 1MHz clock signal RAS which is applied to the two clock inputs of IC620 (pins 10 and 11). This IC contains independent ÷2 and ÷5 counters to produce 500kHz and 200kHz signals as shown in Fig. 4-12. One of these is selected by the data selector, IC622, under the control of the x2 and x5 input lines from the timebase range switch, S61. The output of the data selector, IC622 (pin 9), is applied to IC621 which is an LS1 programmable decade divider. This device divides the input frequency by a number of decades, as

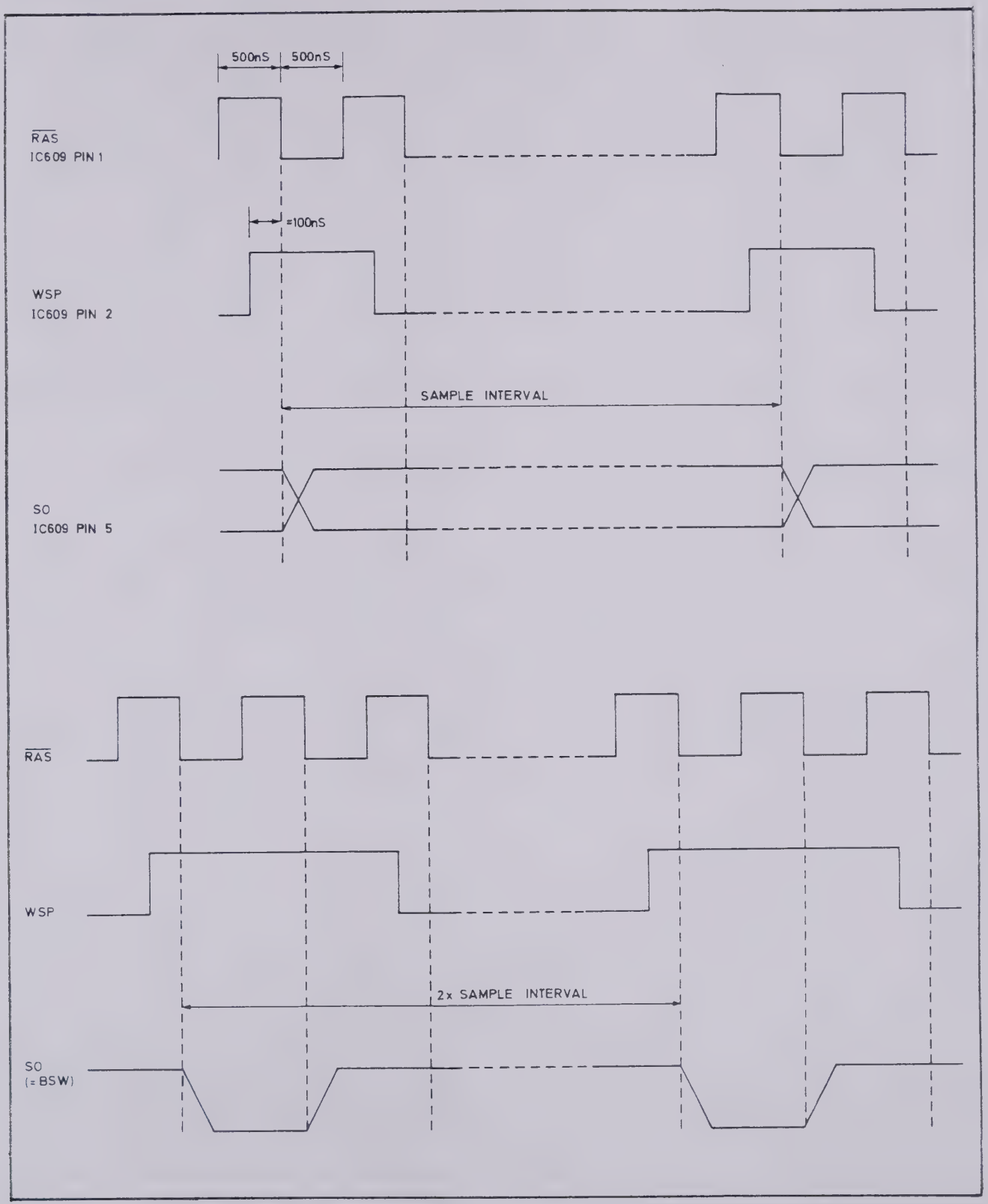


FIGURE 4-11 DELAY STORE ADDRESS COUNTER TIMING A + B

TABLE 4-2 TIMEBASE RANGE DIVIDER CONTROL LINES

TIME/CM Range	WSP frequency (IC602 pin 7)		TIME/CM switch control lines							IC621 Inputs			NOTES
	single trace	dual trace or split trace	x2 (SKN-9)	x5 (N-10)	1ms (N-14)	10ms (N-11)	100ms (N-12)	1s (N-15)	10s (N-13)	10^1 (pin 14)	10^2 (pin 13)	10^4 (pin 12)	
0.1ms/cm	continuously high		1	1	1	1	1	1	1	0	0	0	1. A logic '1' indicates a TTL logic high level
0.2ms/cm	500kHz	250kHz	0	1	1	1	1	1	1	0	0	0	
0.5ms/cm	200kHz	100kHz	1	0	1	1	1	1	1	0	0	0	
1ms/cm	100kHz	50kHz	1	1	0	1	1	1	1	1	0	0	2. The 10^8 input (IC621 pin 11) is permanently low
2ms/cm	50kHz	25kHz	0	1	0	1	1	1	1	1	0	0	
5ms/cm	20kHz	10kHz	1	0	0	1	1	1	1	1	0	0	
10ms/cm	10kHz	5kHz	1	1	1	0	1	1	1	0	1	0	
20ms/cm	5kHz	2kHz	0	1	1	0	1	1	1	0	1	0	
50ms/cm	2kHz	1kHz	1	0	1	0	1	1	1	0	1	0	
0.1sec/cm	1kHz	500Hz	1	1	1	1	0	1	1	1	1	0	
0.2sec/cm	500Hz	250Hz	0	1	1	1	0	1	1	1	1	0	
0.5sec/cm	200Hz	100Hz	1	0	1	1	0	1	1	1	1	0	
1sec/cm	100Hz	50Hz	1	1	1	1	1	0	1	0	0	1	
2sec/cm	50Hz	25Hz	0	1	1	1	1	0	1	0	0	1	
5sec/cm	20Hz	10Hz	1	0	1	1	1	0	1	0	0	1	
10sec/cm	10Hz	5Hz	1	1	1	1	1	1	0	1	0	1	
20sec/cm	5Hz	2.5Hz	0	1	1	1	1	1	0	1	0	1	
50sec/cm	2Hz	1Hz	1	0	1	1	1	1	0	1	0	1	

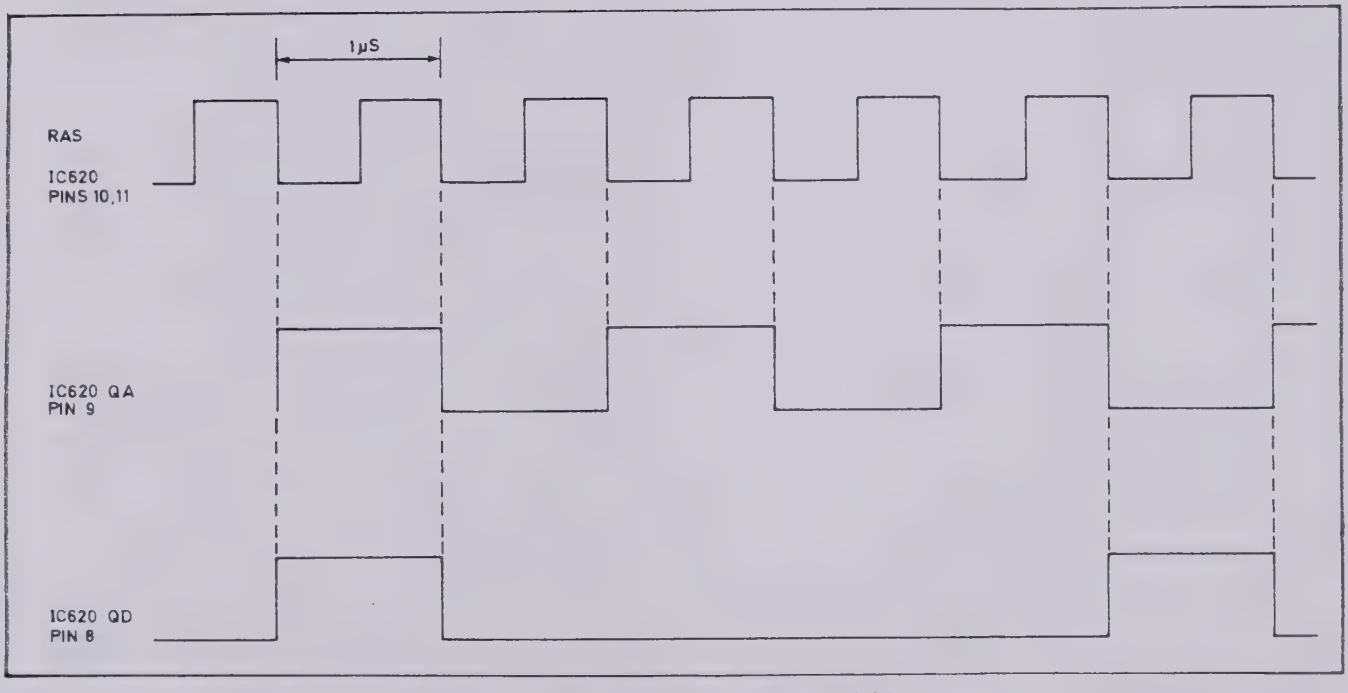


FIGURE 4-12 RANGE DIVIDER WAVEFORM

determined by the four BCD encoded inputs, 10^1, 10^2, 10^4 and 10^8 (pins 14, 13, 12 and 11 respectively). These BCD programming inputs are derived from the timebase range switch decade lines by the gates IC614A, B and C. The state of the timebase range switch and BCD programming lines is shown in Table 4-2 for each timebase range.

The output of IC621 at pin 1 is the basic frequency required for single trace operation. For dual trace operation a further ÷2 is required and this is accomplished by the J-K bistable, IC627A. The direct or divided frequency output is selected by one channel of the quad two input data selector, IC601, and the required output appears at IC601a, pin 12.

The output from the frequency divider chain is fed to the retiming circuitry consisting principally of IC602. For each negative transition of the divider chain output, the retiming circuitry will produce a single WSP pulse lasting 1µs in the single trace mode (single store entry cycle) or 2µs in the dual trace mode (two consecutive store entry cycles: one for each channel). The waveforms associated with the retiming circuitry are shown in Fig. 4-13A (single trace) and B (dual trace).

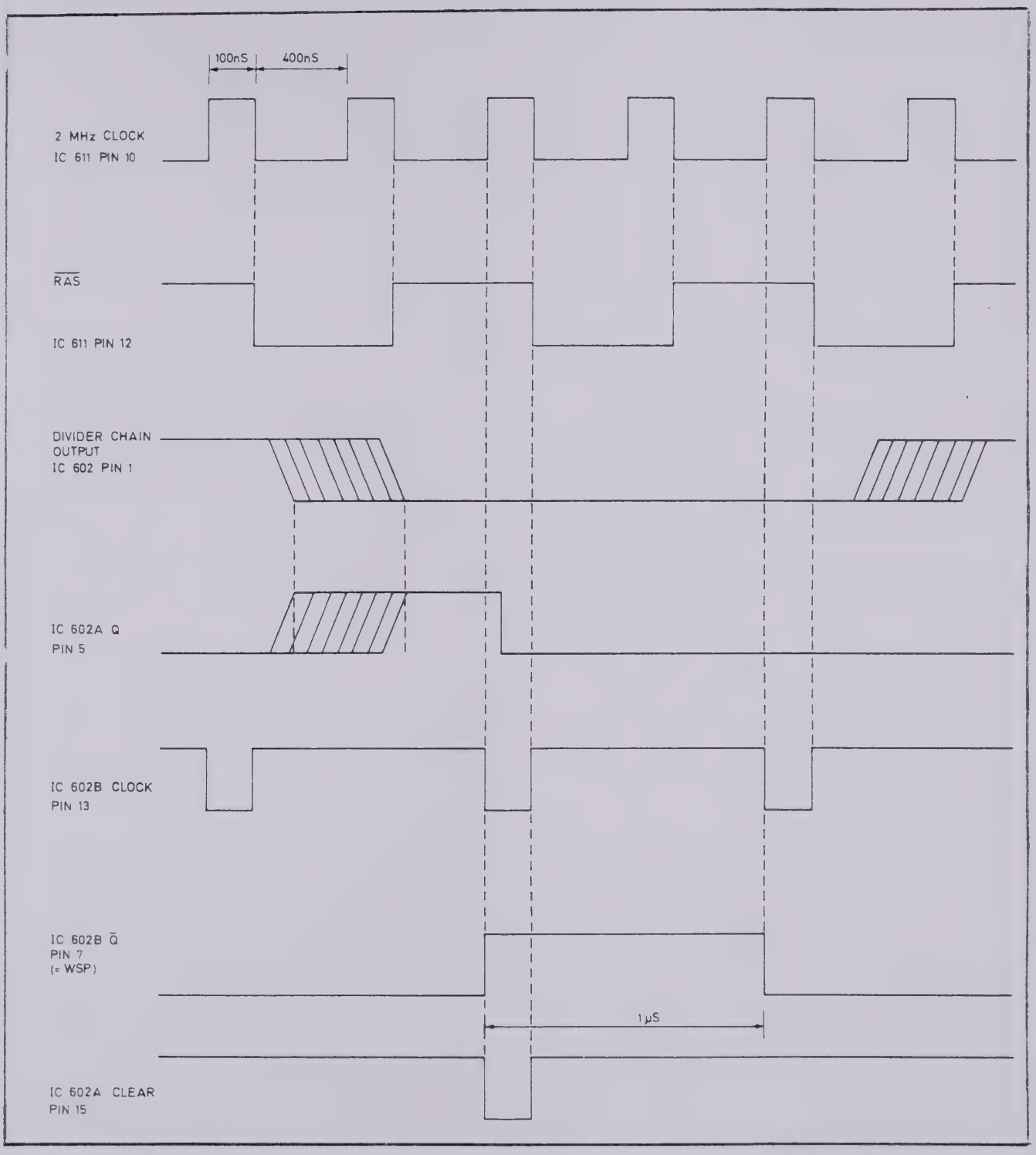


FIGURE 4-13A RANGE DIVIDER RETIMING A

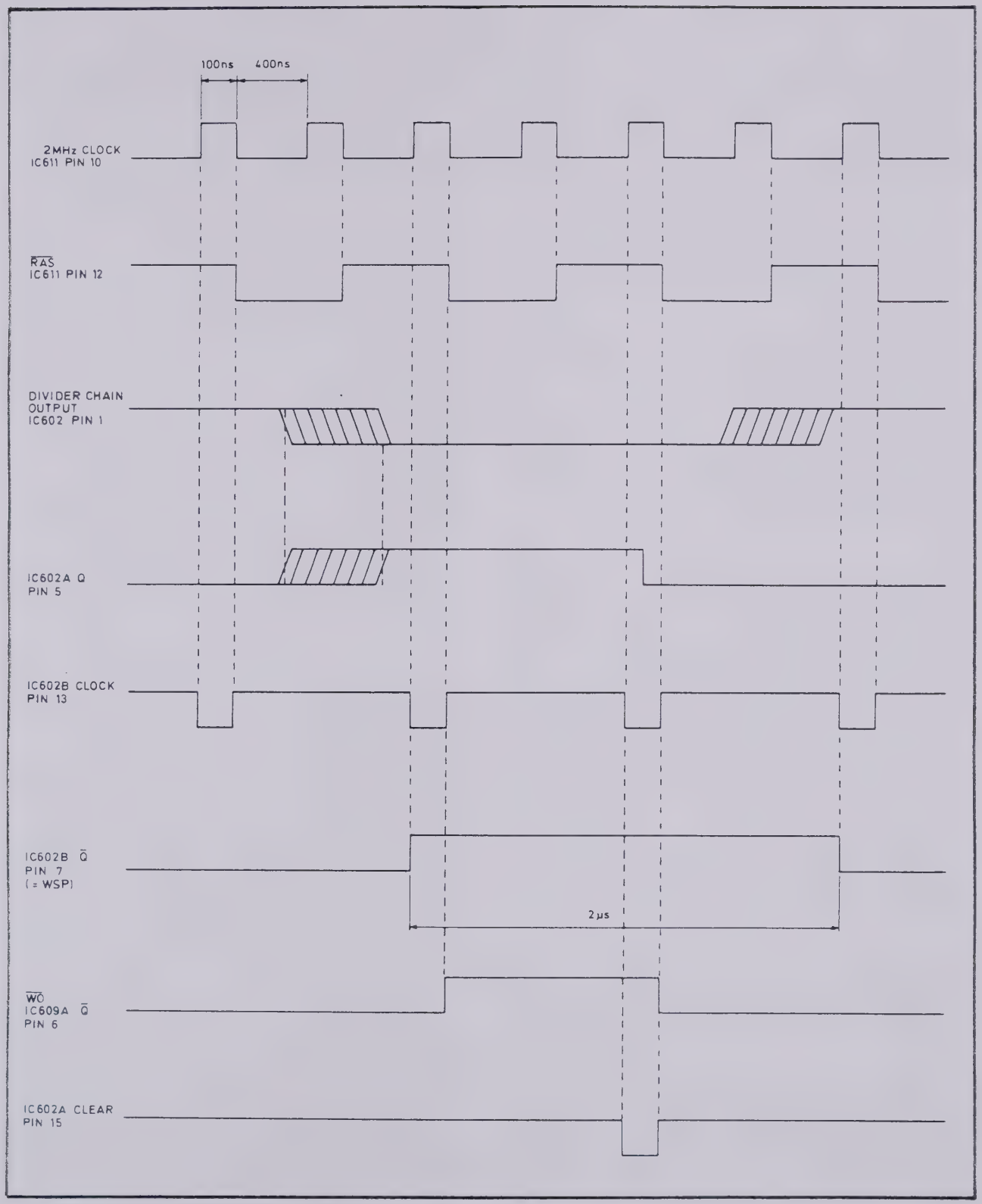


FIGURE 4-13B RANGE DIVIDER RETIMING B

In the single trace mode a negative transition of the frequency divider chain output, which is applied to the clock input of IC602A (pin 1) will cause IC602A Q output (pin 5) to be set to a high level. IC602B is clocked via IC610B with a combination of $\overline{RAS}$ and the 2MHz clock used to generate RAS, thus providing a 1MHz clock signal whose negative going edge precedes the main $\overline{RAS}$ edge by about 100ns. Thus the logic high at IC602A Q output is transferred via the J and K inputs to IC602B $\overline{Q}$ output, approximately 100ns ahead of the negative going $\overline{RAS}$ edge. This output is the write strobe pulse (WSP) signal used to initiate a store entry cycle. The 2MHz clock which is gated with $\overline{RAS}$ in IC610B to provide the clock for IC602B is also applied to an input of IC611B, together with $\overline{RAS}$ and the WSP output. This provides a reset pulse lasting approximately 100ns to IC602A as soon as the WSP output has gone high. Since IC602A is reset in this manner, the WSP output from IC602B will be terminated when the next negative clock edge to IC602B occurs.

Operation in the dual trace mode is similar, except that the inverted delay store least significant bit address, $\overline{WO}$, is also applied to gate IC611B via the data selector IC601. This ensures that the clear pulse to IC602A only occurs when $\overline{WO}$ is high, thereby extending the length of the WSP signal to 2μs and ensuring that a sample from both input channels is recorded in the store during each store entry cycle.

4.4.6 FRONT PANEL CONTROLS

The front panel controls which affect the store and control logic are the timebase range switch, described in the previous subsection, and the 10 pushbutton switches mounted on the store logic PCB (extreme RH side of the instrument) S601 to S610, together with the AUTO TRIGger switch, S512, on the display PCB. Switch debouncing is performed by the two quad latch devices, IC604 and IC605. These latches are continuously clocked by a 50Hz (100Hz in dual trace) signal, obtained from the read address counter, IC628 (pin 8). The 10 or 20ms period between clock pulses allows time for any bouncing action of the switch contacts to cease and thus prevents unwanted multiple transitions. The mode of operation of each of the front panel control inputs is described below:

HOLD (S601)
When S601 is operated one end of R602 is grounded, drawing approximately 10mA through the HOLD LED, D61. A logic low is also latched at the Q3 output (pin 10) of IC604. This logic low is applied to one input of the gate, IC611A, thus disabling the write enable pulses (WEP) to the main store and preventing currently held data being overwritten. Note that the $\overline{RDO}$ line is connected to switch S601 so that when $\overline{RDO}$ goes low to indicate an output plot is in progress (see output option description), the hold function is applied.

SPLIT TRACE (S602)
One contact of S602 also illuminates the HOLD LED, D61, via R602. The remaining contact causes a logic high to be latched at the Q4 output of IC604 and gated with the least significant bit of the write address, WO, at IC603B. Thus whenever WO is in the high state a logic low from the output of IC603B (pin 6) is applied to IC611A to disable the WEP signal to the main store and prevent data in that particular location being overwritten. In the dual trace mode only CH2 samples are written into the "odd" locations (i.e. WO high) and these will be held. note that the logic low that appears at IC604 Q4 when S602 is operated, is applied via D603 to the $\overline{DTH}$ line to indicate that the store information should be read out as two separate traces.

PLOT O/P (S603)
When S603 is pressed a logic low is latched at IC604 Q2 output (pin 7) which is transmitted to the output option (when fitted) to initiate a plot cycle, see section 4.10.

SIGNAL DELAY (S604)
When S604 is pressed a logic high is latched at IC604 $\overline{Q}$1 output (pin 3). This is applied to the select inputs of the data selectors, IC646 and IC649, causing delayed data from the delay stores to be fed to the main store.

ARM (S605)
When S605 is pressed a logic low is latched at IC605 Q4 output (pin 15). This is applied to the clock input of IC612B (pin 13) and arms the timebase when in the single shot mode (see section 4.4.3). Note that operating S605 also applies a logic low via D601 to the D3 input of IC605, and thus the Q3 output at pin 10. Due to the feedback applied between the Q3 output and the D3 input via D602 and S606, the low level at Q3 will remain after S605 is released. The Q3 output is used in the write control logic to indicate that the single shot operating mode is required (see section 4.4.3).

NORMAL (S606)
Pressing S607 removes the latching feedback action described above around the third bistable in IC605, and causes the Q3 output to return to the high state and the write control logic to resume normal repetitive triggering.

MANUAL TRIGGER (S607)
Pressing S608 causes a logic low to appear at IC605 Q2 output (pin 7), thus locking IC613B into the set state via the preset input, pin 10. This simulates a trigger pulse arriving at the clock input and causes a single writing sweep to occur.

± TRIGGER MODE (S608)
Pressing S604 allows the DSL line to the display PCB to go high, thus enabling the window mode trigger circuitry (see section 4.6). The gate, IC606C, is also enabled so that the trigger window 'SET' LED D67 becomes active.

–VE TRIGGER SLOPE (S610)
S610 selects either the incoming $\overline{TR9}$ signal from the trigger circuitry on the display PCB, or its inverse at IC606A, pin 3, as a trigger signal for the write control logic.

4.4.7 READ ADDRESS COUNTER

The read address counter circuitry consists of the 10 bit binary ripple through counter comprising IC623, IC625 and IC628, together with the five phase ring counter, IC616, IC617B and the dual four input data selector, IC615, which determines the operating mode of the address counter.

Although the read address is selected by the main store address selectors (IC630 – IC637) every 1μs during the time the RAS clock is high, the read address itself is only incremented every 10μs. The clock signals for the counter are derived principally by IC616 and the waveforms produced and their relative timing is shown in Fig. 4-14. The 2MHz clock (1) which is used to produce RAS in IC655 is gated with RAS itself in IC610D to produce the 1MHz signal (3) at the output of IC610D (pin 11). Note that the negative going edge of this waveform precedes the negative going edge of RAS by approximately 100ns, and that all the read address waveforms change synchronously with this edge. The output of IC610D is applied to the first stage of the 4 bit counter, IC625, at pin 10 since this stage is not used for the main address counter. Waveform (4) on Fig. 4-14 shows the divided output from IC625, pin 9, at a 500kHz rate, and this is used to clock the four bistables in IC616. IC616 is a quad D type latch with its four stages connected up in a shift register arrangement. Thus the pulse (5) which occurs at its first output is shifted successively through to the other outputs as shown in waveforms (6), (7) and (8). The four input gate, IC617B, detects when all outputs are low (9), and feeds a pulse into the first input of IC616 at pin 4 so that the sequence repeats. Note that because IC617B is an inverting (NAND) gate, the first output from the shift register, IC616, is taken from the $\overline{Q}$ output (pin 3) rather than the Q output, to restore the correct polarity. In this way IC616 produces a five phase 100kHz clock. Only two of these phases are used; that from the Q3 output (pin 10), which is labelled LTX, and from the Q4 output (pin 15), which is labelled LTY.

The read address counter itself is made up of 4 bit counter packages. The 4 stages of IC623 supply the least significant 4 bits of the address R0 to R3. The last three stages of IC625 provide the next three bits, R4 to R6, and the first three stages of IC628 supply the remaining three bits of the read address, R7 to R9. There are three distinct operating modes for the read address counter, viz:-

1. Single trace T-Y mode in which all 1024 store locations are read out in a single sweep at 10μs intervals.
2. Dual trace T-Y mode in which all the 512 CH1 locations are read out in one sweep, and then all 512 CH2 locations in the next.
3. XY mode in which each X (CH1) location is read out together with the corresponding Y (CH2) location in one 10μs interval.

The circuit configuration required for each operating mode is determined by the dual four input data selector, IC615. The read address counter chain is broken after the first stage so that the clock input to the second counter bistable (the stage that produces the R1 address line) is selected by one half of the data selector, while the other half selects a source for the R0 address line. The data selector itself is controlled by two select inputs (pins 14 and 2) which are connected to the $\overline{DTH}$ (low for dual or split trace) and $\overline{XYR}$ (low for XY readout mode) lines. In the single trace mode the R0 address line is connected to the output of the first counter bistable (IC623, pin 9) as is the clock input to the second bistable (IC623, pin 11). The clock input to the first bistable is fed with the LTX pulse from IC616, pin 10, and the read address counter now functions in a conventional mode as shown in Fig. 4-15A. The address is incremented one count on the negative edge of each LTX pulse. The read data from the store is latched on the Display PCB by the rising edge of the LTY pulse which occurs at the same time as the falling edge of the LTX pulse (see Fig. 4-17 and secion 4.5). In the dual trace mode the least significant address line, R0, is held alternately high (CH2 locations) and then low (CH1 locations) for one complete sweep by connecting it via the data selector, IC615, to the QD output (pin 8) of IC628. This is the output of a bistable which is clocked by the most significant address line, R9, and thus toggles at half the overall sweep rate. Since it has the lowest repetition frequency in the read address counter chain, it is used to latch the control inputs in IC604 and IC605 (see section 4.4.6). The clock input to the second stage of the read address counter is connected via the data selector, IC615, to the LTX pulse so that the overall read address in the dual trace mode is incremented in steps of two at 10μs intervals as shown in Fig. 4-15B.

In the XY readout mode the LTX pulse is used as the least significant address line, R0, so that both CH1 (or X) and CH2 (or Y) address are accessed in one 10μs interval. Note that in this mode the data for the X channel is latched on the display PCB on the rising edge of LTX – after the R0 address line has been held low – whereas the Y channel data is latched, as before, on the falling edge of LTX after the R0 address line has been held high. The address counter is connected as for dual trace readout with the address incremented in steps of two.

A flyback blanking pulse is also generated by the read address counter circuitry. At the end of each sweep the most significant address line, R9, resets from a high to low state. This transition clocks the negative edge triggered bistable, IC629B, into the set state. The bistable is reset by the R2 address line going high, via IC617A, as location 4 is addressed on the new sweep. The negative pulse produced by the $\overline{Q}$ output of IC629B at pin 7 is fed to the blanking amplifier for the CRT via the Display PCB (see Fig. 6-3).

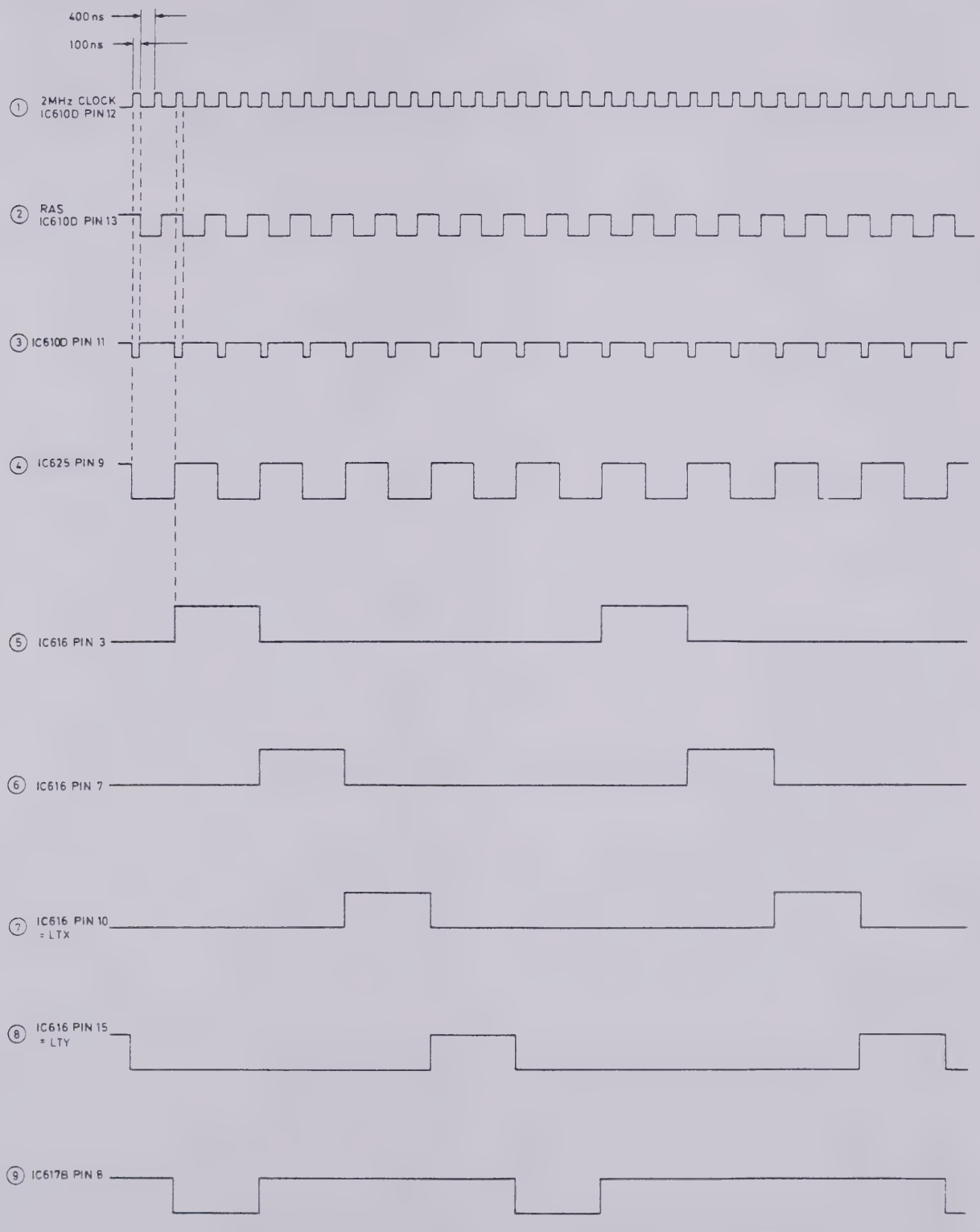

400 ns
100 ns
1 2MHz CLOCK IC610D PIN 12
2 RAS IC610D PIN 13
3 IC610D PIN 11
4 IC625 PIN 9
5 IC616 PIN 3
6 IC616 PIN 7
7 IC616 PIN 10 = LTX
8 IC616 PIN 15 = LTY
9 IC617B PIN 8

FIGURE 4-14 READ ADDRESS COUNTER CLOCK WAVEFORMS

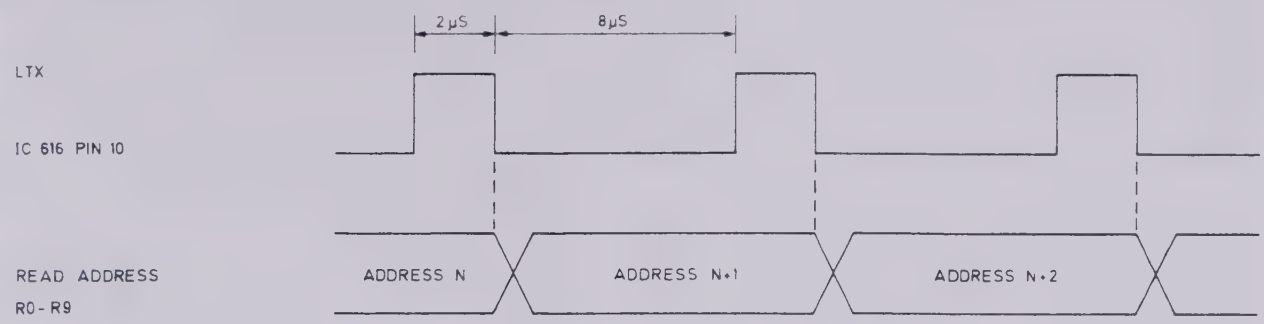


FIGURE 4-15A SINGLE TRACE READ ADDRESS COUNTER MODE

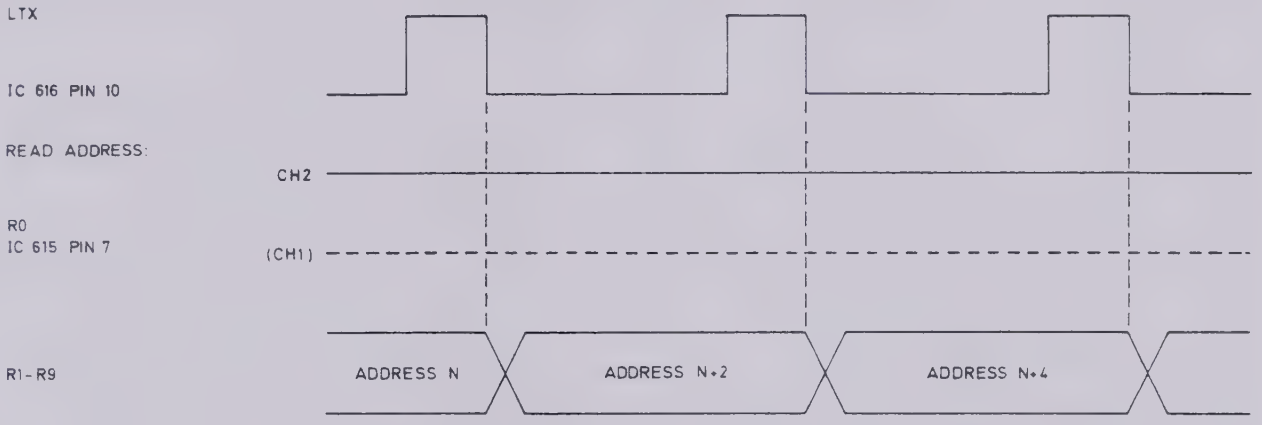


FIGURE 4-15B DUAL TRACE READ ADDRESS COUNTER MODE

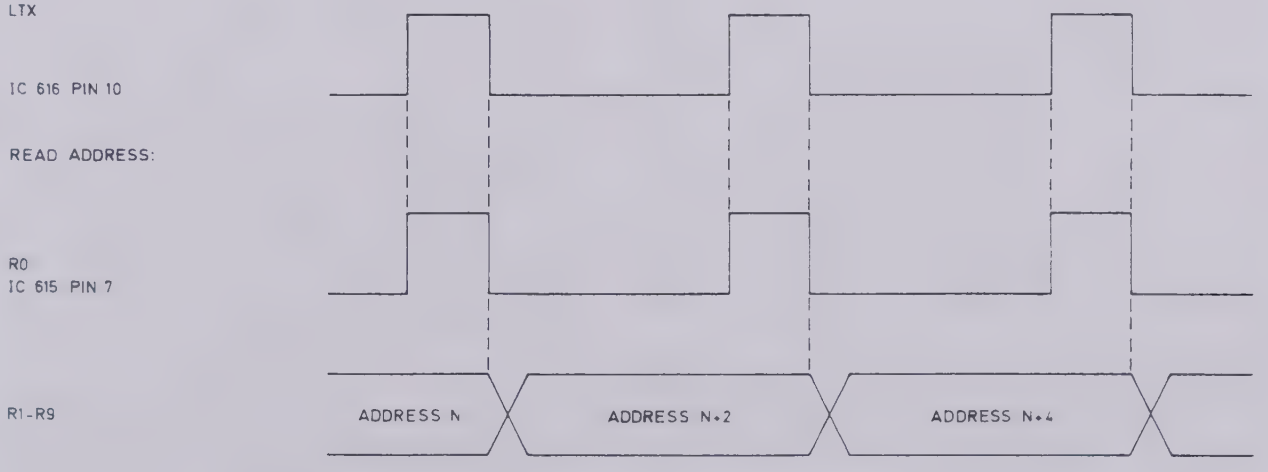


FIGURE 4-15C XY READ ADDRESS COUNTER MODE

FIGURE 4-15 A + B + C R ADDRESS COUNTER MODE

4.4.8 MNEMONIC LIST AND DESCRIPTION INDEX BY IC No.

MNEMONIC LIST

NOTES

1. $\overline{XXX}$ denotes inverse of XXX.
2. All signals assumed to be at TTL levels (see table 2) unless otherwise noted.

Y AMPLIFIER PCB

$\overline{DTH}$ Low if dual trace selected or split trace in operation.

STP ECL levels. Goes high to stop counting in A/D converter.

$\overline{RST}$ ECL levels. Goes low for 50–80ns every 1μs. Resets A/D converter at end of conversion.

BSW Beamswitch signal. High for CH1, low for CH2.

DISPLAY PCB

A0 to A9 see output option when fitted.

D0 to D7 data from store. D0 is least significant bit. D7 is most significant bit.

$\overline{XYR}$ Goes low when XY display mode selected.

$\overline{DTH}$ see Y amplifier PCB.

$\overline{RDO}$ see output option. Normally high.

ATO Goes high when AUTO TRIG selected.

LTX Goes high for 2μs every 10μs: latches X data for DAC.

LTY Goes high for 2μs every 10μs: latches Y data for DAC.

$\overline{SRO}$ see output option. Normally high.

$\overline{ARM}$ see output option. Normally high.

$\overline{STO}$ see output option. Goes low when STORED light is on.

RAS see Store PCB.

$\overline{FYB}$ Goes low for 40μs every 10.2ms in single trace. Goes low for 20μs in every 5.1ms in dual trace or XY. Blanks display when low at end of sweep.

TRG Trigger signal from trigger amplifier.

DSL Goes high when ± slope (trigger window mode) selected.

WEP Goes low for 300ns when data is entered into store.

STORE PCB

RAS 1MHz square wave. Basic clock for control logic.

WSP Goes high when data is to be entered into store.

RST see Y amplifier.

STP see Y amplifier.

X2 Goes low when a '2' range is selected on timebase switch.

X5 Goes low when a '5' range is selected on timebase switch.

$\overline{STO}$ see output option. Goes low when STORED light is on.

$\overline{RDO}$ see output option. Normally high.

$\overline{ARM}$ see output option. Normally high.

$\overline{SRO}$ see output option. Normally high.

BSW see Y amplifier PCB.

TRG see display PCB.

DSL see display PCB.

ATO see display PCB.

D0 to D7 see display PCB.

A0 to A9 see output option.

LTX see display PCB.

LTY see display PCB.

$\overline{XYR}$ see display PCB.

$\overline{DTH}$ see Y amplifier PCB.

W0 to W9 Write address to store. W0 is least significant bit.

R0 to R9 Read address to store. R0 is least significant bit.

S0 to S7 Address to delay store. S0 is least significant bit.

$\overline{SSH}$ Goes low when ARM button is pressed: returns high when NORMAL button is pressed.

4103 OUTPUT OPTION

$\overline{SRO}$ Goes low when 'PLOT O/P' button is pressed.

$\overline{RDO}$ Goes low when output option is reading out.

$\overline{ARM}$ Goes low for 25–40ms at end of automic plot to re-arm timebase.

$\overline{STO}$ Goes low when STORED light is on. Starts automatic plot.

A0 to A9 Readout address to store. A0 is least significant bit.

AUT Goes high when AUTO readout mode is selected.

CTN Goes high when CONTINUOUS readout mode is selected.

The list below enables the relevant section of the circuit description to be found for any IC on the circuit diagram of the Store Control Logic shown in Fig. 6-2.

601	4.4.5
602 (A, B)	4.4.5
603 (A, C, D)	4.4.4
603 B	4.4.6
604	4.4.6

605	4.4.6
606 (ABCD)	4.4.3
607	4.4.3
608	4.4.3
609	4.4.4
610 ABD	4.4.5
610 C	4.4.2
611 A	4.4.2
611 B	4.4.5
612 AB	4.4.3
613 AB	4.4.3
614 ABC	4.4.5
615	4.4.7
616	4.4.7
617 A, B	4.4.7
618	4.4.2
619 not used	
620	4.4.5
621	4.4.5
622	4.4.5
623	4.4.7
624	4.4.4
625	4.4.7
626	4.4.4
627 A	4.4.5
628	4.4.7
629 A	4.4.4
629 B	4.4.7
630	4.4.2
631 not fitted	
632	4.4.2
633	4.4.2
634 not fitted	
635	4.4.2
636 not fitted	
637	4.4.2
638	4.4.2
639	4.4.2
640	4.4.2
641	4.4.2
642	4.4.2
643	4.4.2
644	4.4.2
645	4.4.2
646	4.4.2
647	4.4.2
648	4.4.2
649	4.4.2
650	4.3.2
651	4.3.2
652	4.3.2
653	4.4.2
654	4.4.2
655	4.4.2
656	4.4.2
657 ABC	4.3.2
658 ABCD	4.3.2
659	4.3.2
660	4.3.2
661 A, B	4.3.2
661	4.4.2
662	4.3.2
663 ABCDEF	4.3.2
664	4.3.2
665	4.3.2
666 ABCD	4.3.2
667	4.3.2
668	4.3.2
669	4.3.2

4.5 DIGITAL TO ANALOG CONVERTERS

4.5.1 GENERAL DESCRIPTION

Fig. 4-16 is a block diagram of the digital to analog converters and their associated circuitry. The signal for the Y (vertical deflection) channel is obtained from stored data. The X (horizontal deflection) channel signal may be either stored data (X-Y mode) or a linear sweep (T-Y mode).

The Y channel data latches are loaded with data from the store every 10μs. This is presented to the Y channel DAC (digital to analog converter) and converted into an analog current by a set of eight binary weighted current switches. This current is realised as a voltage by the shunt feedback stage and fed out to the vertical CRT plate drivers.

The X channel is nominally similar except for the inclusion of an extra set of data latches. In the X-Y mode, data must be supplied to each DAC from the store simultaneously. In order to do this, new X data is first loaded into the primary data latches and then transferred into the secondary data latches as the Y data latches are loaded. In the T-Y mode the X channel DAC must provide a horizontal sweep signal and this is provided by making the flip-flops in the secondary data latches count in a binary sequence regardless of the data applied to their inputs. This counting operation is controlled by a reset signal supplied by the read address counters on the Store PCB so that it is synchronous with the Y data. Note that since there are 1024 store locations to be displayed the X channel DAC must have 10 bit resolution (2^{10} = 1024).

Dot joining is provided by placing a simple low pass filter in each channel. Since the time response of the filter in each channel is identical, the CRT spot will always move in a straight line between one data point and the next regardless of the actual filter response itself.

4.5.2 CIRCUIT DESCRIPTION

The circuitry is mounted on the Display PCB and the circuit diagram is shown in Fig. 6-3. Data is latched into the Y data latches, IC514, IC526, under control of the LTY signal from the Store PCB. Note that the most significant bit of the stored data, D7, is inverted. This is corrected after the data latch by using the $\overline{Q}$ output of the most significant bit. An asynchronous clear pin is available on the data latches and this is brought out to a pin labelled 'set zero' at the edge of the PCB. Shorting

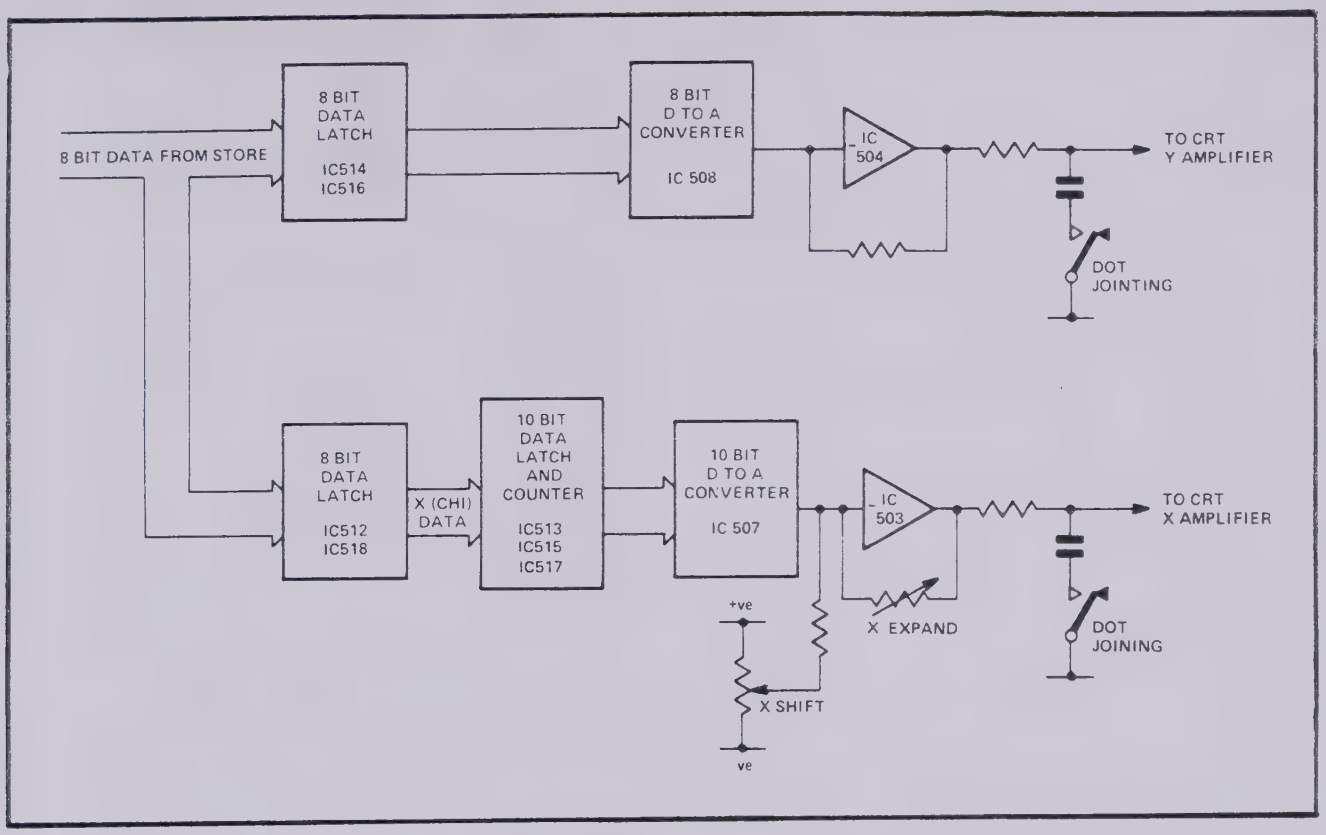


FIGURE 4-16 DAC BLOCK DIAGRAM

this pin to ground causes the DAC to be held at mid-screen level to facilitate setting up adjustments. The X primary data latches, IC512, IC518, are controlled by the LTX signal from the Store PCB, see Fig. 4-17 for timing details.

When the $\overline{XYR}$ line is high (T-Y display mode) IC515, IC513, IC517, form a 10 bit binary counter. The first flip-flops, IC515a,b, are clocked from the negative edge of the LTX signal and the two four bit counters, IC513, IC517, are clocked from the positive going edge of the LTY signal which occurs at the same time. The $\overline{FYB}$ line goes low during the first four data points (first two points in dual trace) nominally to provide CRT retrace blanking. This signal is also applied, via IC510, to the clear inputs of the counter in order to synchronize the ramp produced by the counter.

Note that in the dual trace mode the store is read out as two 512 point traces rather than a single 1024 point trace. Since the data rate is a constant 100kHz the entire store contents take 10.24ms to read out, in either mode. However, in the dual trace mode, two complete sweeps will occur during that 10.24ms and thus the ramp generator rate must be doubled to accommodate this. This is achieved by connecting the preset input of IC515a (pin 4) to the $\overline{DTH}$ line (which goes low during dual trace readout), thus locking its output permanently high and causing the succeeding flip-flop, IC515b, to count once every clock edge instead of every second clock edge.

In the XY display mode the $\overline{XYR}$ line goes low causing IC515 to be held in the cleared state. The clear is removed from IC513 and IC517 however and the load enable inputs (pin 9) are taken low so that the devices function as latches. Since the data coming from the store has only 8 bit resolution, the two least significant bits of the 10 bit DAC, IC507, are held continuously low by IC515.

Both the X and Y channel DAC's, IC508 and IC507, are monolithic devices containing binary weighted current sources, current switches and summing circuitry. IC507 has an internal precision voltage source available at pin 2 and this is buffered by the voltage follower op-amp, IC506, and used to provide a reference current input for the Y channel DAC, IC508, via R554. Both DAC's provide a current sinking output of approximately 2mA full scale and these are applied to virtual earth connected op-amps, IC504, IC503, to provide output voltages of approximately ±0.5 volt full scale. The Y channel op-amp, IC504, has a single feedback resistor, R540, to set the gain. In the X channel, the feedback resistor consists of R549, R541 and the parallel network of R502, R507 and R52. When the XY mode is selected, S502 closes so that only R549 is in circuit and the stage is identical to the Y channel. In the T-Y mode with S502 open, R541 is introduced to increase the scan width from 8.5cms (similar to the Y channel) to 10.2cms, and R52 can increase the gain up to X10 as the X EXPAND control. The parallel network, R502, R507, determines the relative

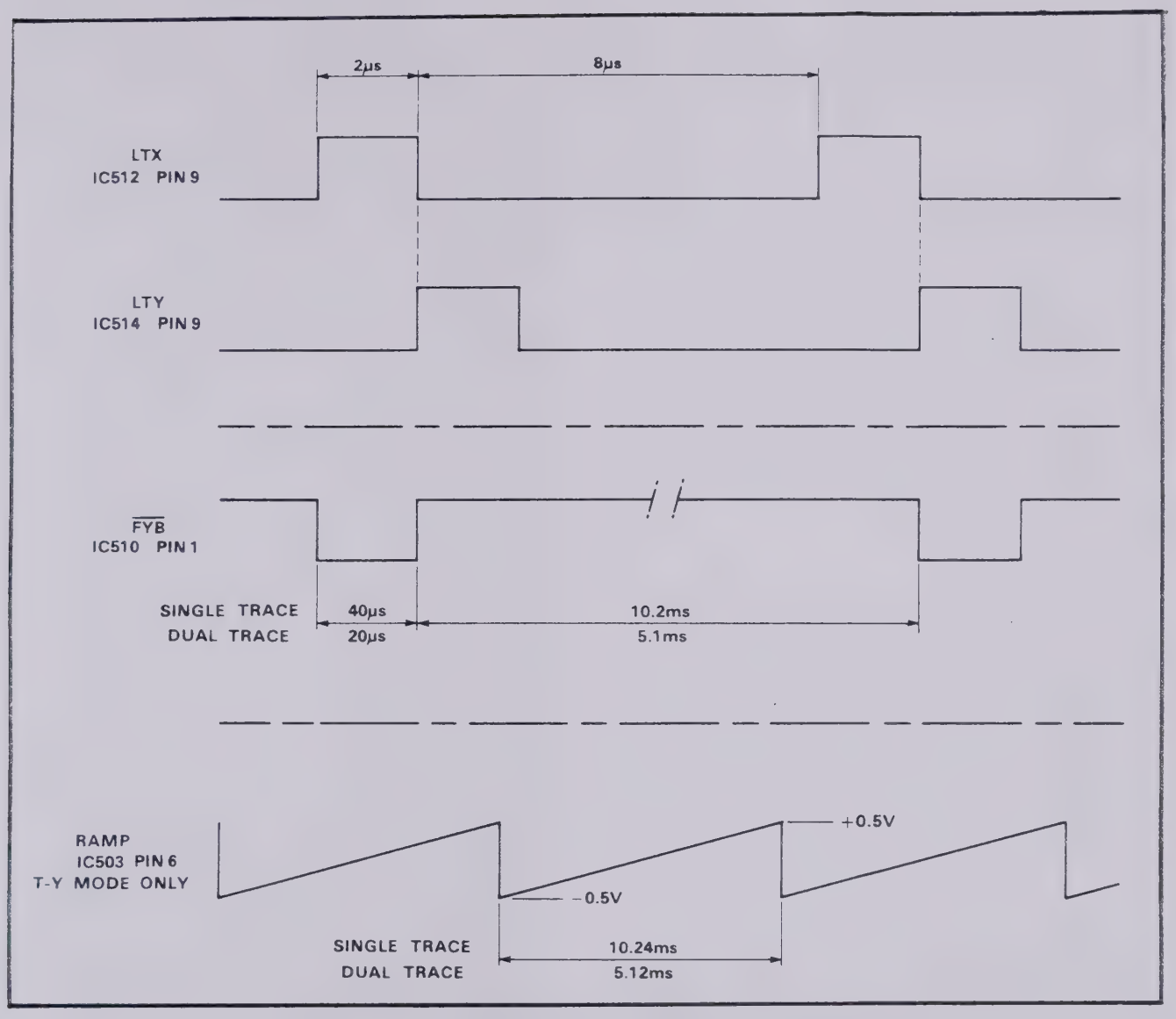


FIGURE 4-17 DAC TIMING

calibration in the fully expanded position. The protection diodes, D510–D513, limit the maximum voltage swing developed during fully expanded operation. Note that both amplifier stages have offset current injection via R553, R556 (Y channel) and R555, R552 (X channel) so that their output voltages swing symmetrically about 0 volts, i.e. 0 volts represents the center of the CRT screen. In addition the X channel has a variable shift introduced via R546, R547, R548 from the coarse and fine X SHIFT controls, R51. This shift is switched out during XY operation by S502.

Dot joining is performed by simple low pass filters in each channel – C504, C505, R542, R543 and C502, C503, R544, R545. When dot joining is switched on the only blanking (Z mod) applied to the CRT is retrace blanking derived from $\overline{\text{FYB}}$ via IC510a. If dot joining is not used the LTY pulse is also used for blanking via IC509a, so that the beam is blanked for 2µs following each new data point appearing to allow the deflection plate driver amplifiers time to settle.

4.6 TRIGGER AMPLIFIER

The trigger amplifier circuitry is located on the Display PCB and is shown in Fig. 6-3. The trigger signal source is selected by switches S508 to S511 and the coupling mode by switches S504 to S507. In the DC coupling mode a direct signal path is established via R503. In the AC coupled mode the signal is passed through C508 and C507 in parallel, blocking any DC voltages but with no significant effect at signal frequencies. The LF REJECT switch is a dummy switch with no contacts and, when selected, the signal passes through the small value capacitor, C507, attenuating trigger signals at frequencies below 1600Hz. The HF REJECT switch, S507, is switched

independently of the others and inserts a low pass filter consisting of R507 and C510 into the signal path.

The filtered trigger signals are applied to the amplifier, IC501, which is arranged in a non-inverting configuration with a gain of approximately five. The protection diodes, D501, D502, limit the signal excursion at the input, pin 3, to about ± 1 volt. Summed into the inverting input of this amplifier via R521, is the trigger level voltage from the potentiometer R54. Thus the trigger signal appears at the output, pin 6, with the trigger level voltage subtracted from it, and is applied to the two comparator circuits, IC502a and IC502b. These devices are differential input comparators with TTL level outputs, and function as Schmitt trigger devices due to the positive feedback applied via R531, R527 and R532, R526 respectively. In the conventional single trigger point mode, only IC502b is active and IC502a is disabled by a TTL low level at the strobe, pin 13. Whenever the input signal from the trigger amplifier crosses zero, the comparator output at pin 10 changes state in the same sense and this output is sent to the control logic on the Store PCB via the buffer gate, IC510b. Note that trigger signal slope selection (+ or – ve) is performed on the Store PCB at TTL levels.

In the Trigger Window mode the DSL line goes high and both comparators become active. The outputs of both comparators are commoned so that either of them may provide a trigger signal. Note that the trigger signal from IC501 is applied to the non-inverting input of IC502b and the inverting input of IC502a so that IC502b detects +ve slope signals and IC502a detects –ve slope signals. In addition, when DSL goes high, diode, D503, is reverse biased, allowing the base of TR501 to assume a positive potential between +0.6V and +4V, as determined by the setting of the TRIGGER WINDOW potentiometer, R53. This injects an offset voltage from TR501 emitter via R524 and R528 into the two comparator inputs, the sense of this offset adding to the input signal to IC501a and subtracting from it for IC501b. Thus the actual trigger level points for each comparator are offset above and below the mean trigger level, producing the trigger window effect shown in Fig. 3-1.

4.7 OUTPUT AMPLIFIERS

The X and Y output amplifiers have different gains but identical circuit configuration. Consequently, only the Y amplifier stage will be described.

The amplifier has a differential input from the display board via R441 and R461 and a differential output to the tube via the collectors of TR407 and TR411.

TR408 and TR409 form a compound NPN transistor with a very high gm. Transistors, TR412 and TR413, are connected similarly. These two compound transistors are connected as a long-tailed pair with R445 and R455 defining the quiescent current and R447 and R449 controlling the gain of the stage. Transistors TR407 and TR411, connected in the common base configuration are current driven from the compound transistors (cascode connection). The output signal voltage is taken from the collector load resistors, R443 and R458.

4.8 CALIBRATOR

The calibrator consists of a square wave oscillator with an accurate 1:1 mark-space ratio, followed by a switched current driving an accurate load resistor.

IC401 is connected as an oscillator with frequency defined by R476, R477 and R462, R471, C419. TR410 is connected as a stable current source which may be switched off by R456 and D408 when IC401 output is low. When the latter is high D408 is reverse biased and thus does not affect the transistor current. The collector current of TR410 flows into R438, an accurate 1kΩ resistor. Thus when the voltage across it is set at 1V, the current through it is 1mA, which is available as a calibration signal by shorting the calibrator output pin to earth.

4.9 POWER SUPPLIES

4.9.1 GENERAL

As shown in Fig. 6-4, the mains transformer, from which all supplies are derived, has two primary windings, one tapped, switched by S3 and S4 to allow for line voltages of 100, 120, 220 and 240V. The frame of the oscilloscope may be switched directly to ground, or isolated by use of S1. In the isolated position, the frame of the oscilloscope is connected to mains ground via the high value resistor, R1 and bridge BR1. The bridge provides operator safety and ensures that the frame of the oscilloscope cannot be taken to a voltage greater than plus or minus two diode drops from ground.

4.9.2 LOW VOLTAGE SUPPLIES

Each of the four low voltage supplies (+5V, –5V, +12V and - 12V) is derived from a floating secondary winding on T1. Each output is full wave rectified, smoothed and passed to a three terminal IC regulator, which produces the required stablization and current limiting. Diodes, D414 to D416, prevent the IC outputs from being taken significantly negative with respect to their common terminal which would be potentially destructive.

The +5V regulator is followed by an over-voltage crowbar, incorporated to protect the logic in case of failure of IC404. Should the output of IC404 exceed approximately 6.5V, D409 will conduct and fire SCR400, which will, in turn blow fuse, FS400.

4.9.3 HIGH VOLTAGE SUPPLIES

See also Fig. 28

The other supplies required by the instrument are derived from the EHT inverter. The +170V supply is derived by forward conversion, the –1500V supply is derived by energy storage. The +4,500V output is produced from the 1500V a.c. output by multiplication.

IC400 is configured as an astable multivibrator whose output, pin 3, drives the power transistor, TR406. The off time is fixed and the on time is defined by time

constant, C404, R429 and also the current injected through R428 and D403, the latter current being a feedback signal.

When TR406 turns on, pin 4 of T400 rises to slightly greater than +170V, charging C410 through D405. This voltage is further smoothed by R435 and C412 to produce the +170V supply. Also during the on time of TR406, energy is stored in T400. When TR406 is turned off, pin 2 of T400 flies negative, and the stored energy is delivered via D300 to C301 to produce the −1500V supply. A feedback signal is derived from R414 in the focus chain by comparing a fraction of the −1500V with the +12V supply and using the resultant error signal to control the on time of the multivibrator, thus establishing a closed feedback loop. The voltage on T400, pin 2, which swings from +1500V to −1500V, also drives a conventional voltage multiplier consisting of D301−303 and C302−304. The resultant signal appearing at the cathode of D301 is further smoothed by R300 and C300 to produce the +4,500V supply used for the final anode, A4.

Components, L400, L401, L403, L404, C408 and C411 provide filtering to avoid the oscillator supply current affecting the low voltage supplies.

The cathode voltage is fixed at −1400V by D400 while grid, G1, is maintained at a more negative voltage, as set by intensity preset, R412, and the front panel INTENSITY control, R400. TTL blanking signals are amplified by TR404 and superimposed on the G1 voltage via C402. D401 d.c. restores the blanking waveform to be negative with respect to the quiescent grid voltage. The anode potential, A2, is set by R402 to optimize focus. Small positive voltages set by R401 and R413 are applied to the third anode and the interplate shield respectively to minimise raster distortion.

4.9.4 GRATICULE ILLUMINATION

The graticule is illuminated by two lamps, LP40 and LP41. Power for these lamps is supplied from the −5V supply controlled by R404 and emitter follower, TR402.

4.9.5 TRACE ROTATION COIL

A coil fitted around the neck of the CRT and inside the magnetic shield is used to align the trace with the horizontal graticule lines. The current required for this is supplied from transistors, TR400 and TR401, adjusted by front panel TRACE ROTate control, R403.

4.10 OUTPUT OPTION 4103

4.10.1 GENERAL

The block diagram of the output unit is shown in Fig. 4-18. A ten bit counter under the control of the PLOT SPEED switch provides addresses to the main store and also the input to the X D.A.C. to produce a ramp output. The data from the main store is latched and passed to the two Y channel D.A.C.'s. The timing logic controls the three plot modes and also the latches which separate CH1 data from CH2.

4.10.2 X - COUNTER

The counter consists of two four-bit counters, IC800 and IC802, and two toggling bistables, IC806(b) and IC803(b), connected as a binary ripple-through counter. The least significant bit is modified when the oscilloscope is in the dual trace mode to accommodate simultaneous sampling. The change is performed by IC809 as described below.

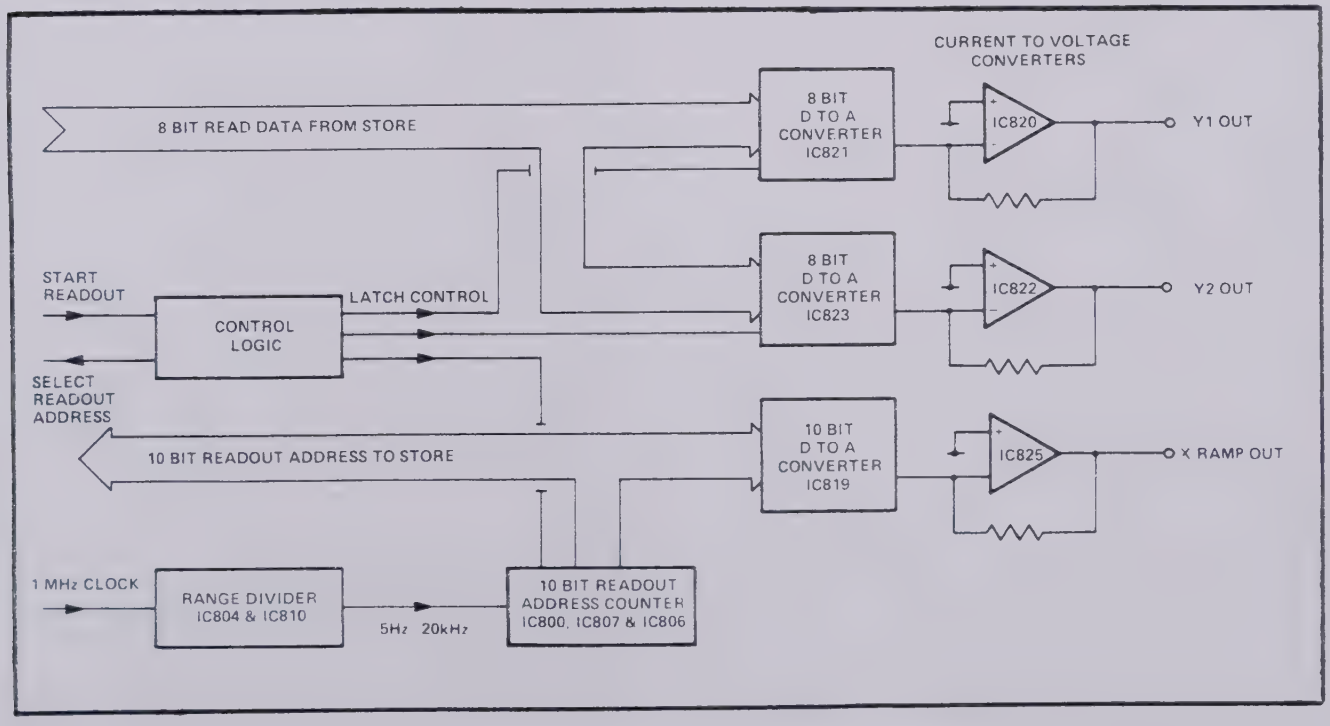
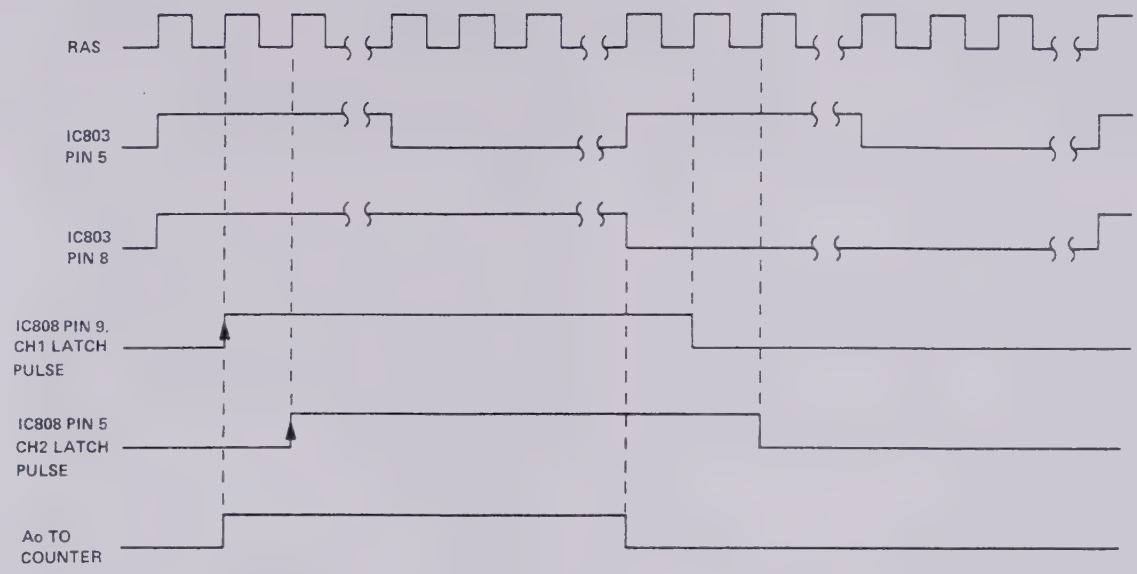
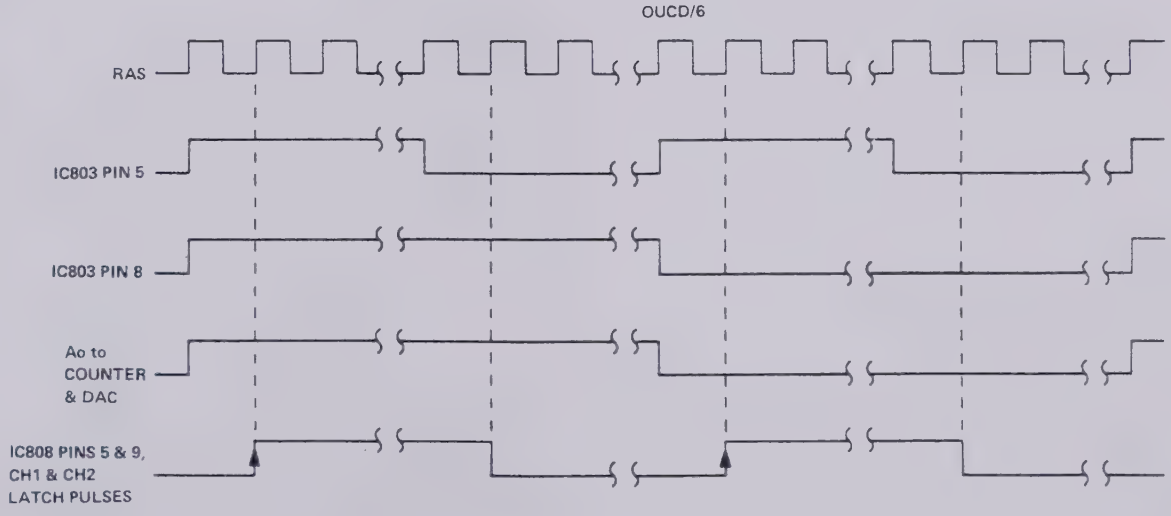


FIGURE 4-18 OUTPUT UNIT BLOCK DIAGRAM



DUAL TRACE OPERATION TIMING WAVEFORMS



SINGLE TRACE OPERATION TIMING WAVEFORMS

FIGURE 4-19 OUTPUT UNIT TIMING WAVEFORMS

5.1 GENERAL

This instrument may be operated at nominal line voltages of 110V, 120V, 220V and 240V, selected by two back panel slide switches (see Section 3.1). In operation, it is protected by two fuses, as follows:-

1. The supply line fuse, FS1, mounted on the rear panel by the line voltage selector switch. The fuse rating is 1/2 Amp slo-blo (Part No. AD-233685) for 220/240V supplies and a 1A slo-blo (Part No. AD-234790) for 100/120V supplies.
2. The +5V fuse, FS400, located on the power supply board, fuse rating 1A (Part No. AD-252162). Access is by removing the bottom cover.

   NOTE: As this fuse provides over-voltage protection from the +5V supply, the latter should be checked before replacing the fuse (see Section 5.3.2).

If a fault cannot be cleared, it is recommended that the instrument be returned to the manufacturer for repair. When faults have been cleared, it is recommended that the calibration procedure be implemented to ensure that the instrument conforms to specification.

5.2 MECHANICAL ASSEMBLY

5.2.1 LAYOUT

WARNING: DISCONNECT FROM THE SUPPLY BEFORE REMOVING COVERS OR ANY INTERNAL ASSEMBLIES. BEWARE EXPOSED HIGH VOLTAGES WHEN OPERATING WITH THE COVERS REMOVED.

Figure 5-1 is a schematic of the internal layout of the instrument and shows the preset controls with sidebars and top/bottom covers removed. Full access to nearly all the preset controls is obtained by removal of the covers only. Each cover is retained in position by four latch fasteners, which may be released by rotating one quarter turn anti-clockwise. When correctly latched, the arrow on the fastener will point towards the corresponding end-frame. For ease of location, the components are coded as follows:-

1–99	:	Mainframe
100–199	:	Y-Amplifier CH1
200–299	:	Y-Amplifier CH2
400–499	:	Power Supply
500–599	:	Display Board
600–699	:	Store Board
800–899	:	Output Option 4103 (when fitted).

The Y-amplifier is an easily removeable sub-assembly, mounted to the left of the C.R.T., operable outside the instrument if required. The two amplifier channels are identical, with corresponding components numbered 1XX on Channel 1 and 2XX on Channel 2.

The power supply board is secured underneath the C.R.T. It contains the low voltage supplies and the E.H.T. inverter producing the high voltage supplies. It also contains the X and Y C.R.T. drive amplifiers and the calibrator.

The cathode rectifier/capacitor and the E.H.T. multiplier are contained in a screened box attached to the main board.

The timebase, mounted to the right of the C.R.T., is another easily removeable sub-assembly, which is also operable outside the instrument if required. The sub-assembly consists of three boards – the store board, the display board (incorporating the trigger circuitry) and the output option (if fitted). The store board is mounted by a hinge, which allows access to both sides of all boards when opened out.

The following details the removal of the individual assemblies and metalwork:-

5.2.2 SIDEBARS

Each sidebar is secured to the instrument by one screw in each end-frame. When these screws are removed, the side-bard with the handle attached may be slid to the top of the instrument and removed.

5.2.3 TUBE

Removal of the tube is straightforward and affords access to the track side of the power supply board. The tube is removed, together with its magnetic shield, in the following manner:-

1. Disconnect the trace rotation leads at SK1 on the power supply board.
2. Remove the tube base cover, which is secured to the back panel by four screws, and carefully disconnect the tube base connector.
3. Remove the two screws connecting the two halves of the tube clamp.
4. Slide the tube backwards until the face-plate disengages from the plastic moulding inside the front cover.
5. Lift the front of the tube and disconnect the E.H.T. lead at the cavity cap connector. Disengage the rotation coil leads from the board. Withdraw the tube, complete with shield.
6. The tube is a push fit inside the magnetic shield and is removed, if necessary, together with the rotation coil.
7. Refit by the reversal of the above procedure.

5.2.4 Y AMPLIFIER

If the sidebars have been removed, the attenuator screen may be removed by removing the four fixing screws. Otherwise, it must be removed with the Y-amplifier, as follows:-

1. Disconnect SKE at the rear of the board.
2. Remove the four screws indicated in Figure 5-1 securing the board to the bulkhead. (View on Y-Amplifier.)
3. Remove the four screws indicated in Figure 5 securing the board to the bulkhead.
4. The assembly may now be withdrawn from the front of the instrument.
5. Remove the two remaining screws securing the atten-uator cover.
6. If required, the amplifier may be operated outside the instrument (with some loss of screening) by replacing SKE.

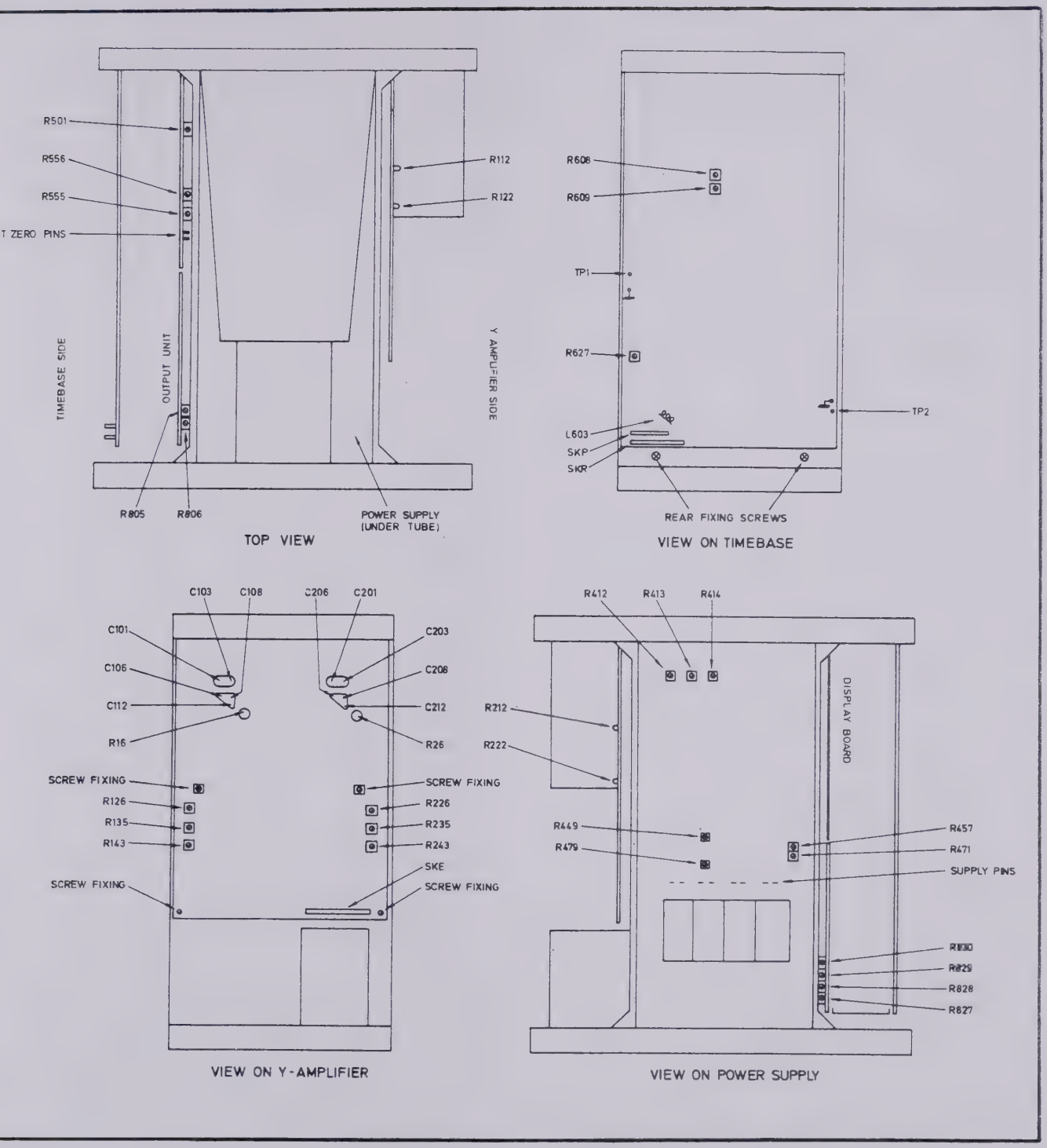


FIGURE 5-1 PRE-SET CONTROLS LOCATION

5.2.5 POWER SUPPLY

As mentioned in Section 5.2.3, access to the track side of the power supply board is obtained by removing the tube. Access to the E.H.T. oscillator components is obtained by removing the two screws fixing the E.H.T. box to the main board and lifting the box as far as the connecting wires will permit. When refitting the box, coil these wires under the potted half of the box.

5.2.6 TIMEBASE ASSEMBLY

This assembly is removed as follows:-

1. Disconnect sockets P and R at the back of the store board.
2. Remove the four screws securing the front panel to the end-frame.
3. Remove the two screws securing the assembly to the bulkhead indicated in Figure 5-1 (View on Timebase.)
4. The assembly may now be withdrawn from the front of the instrument. The assembly must be removed straight as damage may occur if components are knocked against the front frame.
5. Remove the three screws securing the store board to the upper (square) bar of the assembly. Slide the store board back until the push-buttons clear their bezels. The store board may now be hinged away from the assembly chassis.
6. If required, the timebase may be operated outside the instrument by re-connecting sockets P and R.
7. Refitting is the reverse of the above procedure. When the store board push-buttons are slid into their bezels, it is possible that a few of the latter may be displaced. They are, however, a snap fit and should simply be pressed back into place.

5.2.7 FITTING AN OS4103

To fit an OS4103to an existing OS4100, proceed as follows:

1. Remove the screw and ground terminal securing the blanking plate on the rear mainframe behind the timebase assembly. Discard the plate and refit the ground terminal.
2. Remove the top and bottom covers of the oscilloscope as detailed in section 5.2.1.
3. Remove the timebase assembly as in section 5.2.6, steps 1 to 4.
4. Unscrew and remove the rear plate of the timebase assembly, retaining the four screws.
5. Remove the screws holding the two OS4103 rear plates together without separating the latter.
6. Attach the plates to the rear of the timebase assembly as shown in Fig. 5-2 using the original four screws.
7. Fit the OS4103 circuit board, with screws through the four spacers provided.
8. Release the free ends of cables T and U from their protective foam and insert them into sockets T and U on the display board as if Fig. 5-1, taking care not to bend any of the pins.
9. Reconnect the timebase assembly. Check the operation of the output unit and recalibrate if necessary as in section 5.3.9.

5.3 CALIBRATION PROCEDURE

The calibration procedure is shown below. Note that calibration should not be attempted until the instrument has been allowed to warm up for at least 15 minutes. Refer to Figure 5-1 for the location of preset components.

5.3.1 TEST EQUIPMENT REQUIRED

1. Multimeter to measure up to 1500V, with at least 20kΩ/volt input impedance. Accuracy to be within ±2%.
2. Function generator, preferably with triangle wave output.
3. D.V.M. with 3½ digit display and accuracy within ±0.2%.
4. Source of time and voltage calibration signals to cover range 0.1mV to 40V, 1kHz time markers.
5. Capacitance standardizer, 1MΩ/28pF, with BNC connections.
6. Digital frequency meter to give a resolution of 0.1% or better at 1kHz and 1MHz.
7. Dual trace oscilloscope, with 100nsec/cm range.

5.3.2 POWER SUPPLY VOLTAGES

All voltages measured on power supply board.

1. Set the supply voltage switch to suit the available supply.
2. Check the supply voltages at the pinheads in front of the large electrolytic capacitors –

	Min.	Max.
pin (32) with respect to pin (34)	4.75V	5.25V
pin (38) with respect to pin (36)	–4.75V	–5.25V
pin (26) with respect to pin (27)	11.4V	12.6V
pin (29) with respect to pin (27)	–11.4V	–12.6V

3. Measure the voltage at the end of R472 nearest the bulkhead with respect to the chassis. It should be within the range 155V to 185V.
4. Measure the voltage across R410.

CAUTION – BOTH ENDS OF THIS RESISTOR ARE AT GREATER THAN – 1kV FROM CHASIS VOLTAGE.

Adjust R412 such that the voltage across R410 does not exceed one volt when the intensity pot is turned fully clockwise. This limits the maximum available cathode current.

5. Measure the cathode voltage at one end of R410. It should be between –1330V and –1470V with respect to the chassis, adjusted if necessary by R414. The

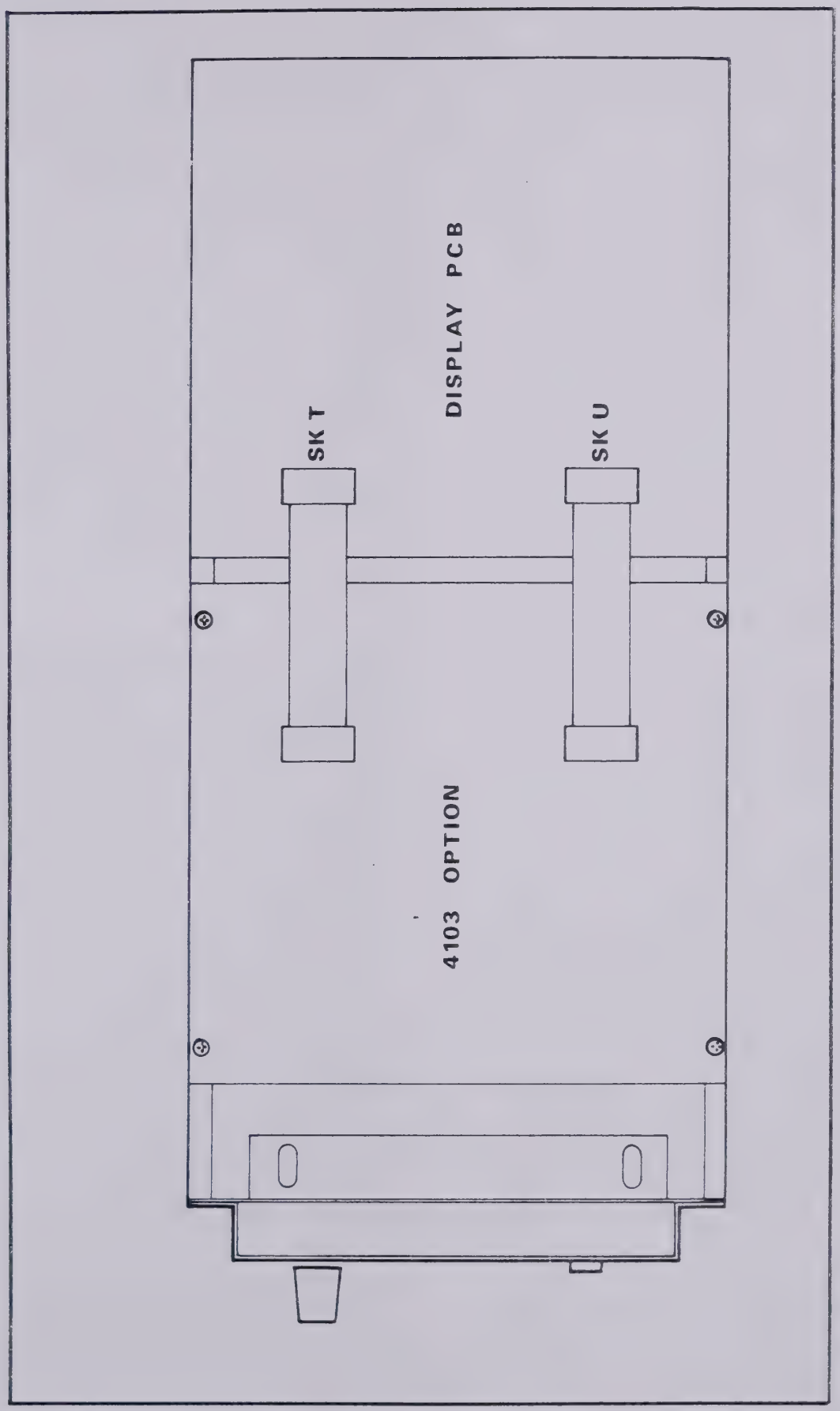


FIGURE 5-2 OS4103 FITTING

cathode voltage should vary by less than 1% when the intensity control is turned from minimum to maximum.

5.3.3 GEOMETRY

1. Set the TIME/cm switch to 1msec/cm, select AUTO TRIGger and T-Y. Push the NORMAL button if trace is stored, ensure both 'hold' buttons are released.
2. Select CH1 and GND. Using the shift control, obtain a trace near one of the graticule lines. Adjust FOCUS and ASTIG controls for clear picture. Adjust the TRACE ROTATE preset on the front panel to produce a trace parallel to the graticule lines.
3. Shift the trace alternately to the top and bottom of the screen, while adjusting R413, the geometry pot on the power supply board, to minimise trace distortion.
4. Select CH2 also and connect a triangle wave of approximately 1kHz to the CH2 input. Adjust the sensitivity for an approximate 8cm pk-pk trace.
5. Switch to X-Y mode. Check the distortion at the left and right of the screen using the CH1 (X) shift control. If necessary, readjust R413 to obtain a compromise between horizontal and vertical.
6. Return to T-Y, CH2 only. Adjust FOCUS and ASTIG controls for optimum trace quality.

5.3.4 TIMEBASE

1. Using a digital frequency meter, measure the frequency of the signal appearing at TP2 on the logic board. This should be adjusted to 1MHz ± 1% by altering the inductance of L603 when required. Reducing the separation between turns decreases the frequency. Only small physical adjustments should be required.
2. Set the TIME/cm switch to 0.1msec/cm and select auto-trigger. Connect one channel of an oscilloscope to TP1 on the logic board and another channel to TP2. Trigger on the negative going edge of the waveform on TP2. The required waveforms are shown (Fig. 5-3). T_1 may be set to 100nsec by adjustment of R609 (center of the logic board). Note that this will also affect T_2. T_2 can be brought to 100nsec by adjustment of R608. As these presets are masked by the sidebar, this may be removed (see Section 5.2.2). Alternatively, the timebase may be removed and operated outside the instrument.
3. Set the TIME/cm switch to 1msec/cm. Select CH1 only, trigger on CH1 and connect a sine/triangle wave signal of approximately 200Hz to the CH1 input. Adjust the trigger level and attenuator controls to give a stable trace, with the signal limiting at the top and bottom of the screen. The signal should limit cleanly at the bottom of the screen and be free of major uncertainties over the entire Y-range. If this is not the case, it will be necessary to adjust R627 such that:

   a) It is as far clockwise as possible, consistent with clean limiting at the bottom of the screen.

   b) It is set approximately midway between two of the settings that produce excessive uncertainty on the trace (there are several of these on the complete rotation of R627).

5.3.5 DISPLAY

1. Switch the display to X-Y and connect together the two 'set zero' pins (at the middle of the top edge of the display board) with a crocodile clip or screwdriver blade. This will produce a single dot, regardless of signal inputs, which must be brought to the exact center of the screen by presets R556 (Y) and R555 (X) on the top edge of the display board. Disconnect the two pins and return to T-Y display.
2. Set TIME/cm control to 1msec/cm and X-EXPAND to X1. Apply 1ms markers to CH1 and trigger on positive edge. With very narrow marker pulses, the use of the filter will produce a more stable display. Adjust R479 on the power supply board for 1cm between markers.
3. Turn X-EXPAND control to X10 and adjust R501 on the display board for 10cm between marker pulses. Return the EXPAND control to X1.
4. Set the TIME/cm control to 2msec/cm, apply a sine wave of approximately 50Hz to CH1 and adjust for an 8cm trace. Ensure that only CH1 is selected. Switch to X-Y display. This will display a diagonal line, whose slope must be set to 45° by R449 on the power supply board.

5.3.6 Y-AMPLIFIER

1. Select CH1 with input grounded and AUTO TRIGger. Set TIME/cm switch to 1ms/cm and CH1 attenuator switch to 1mV/cm. Adjust the front panel BALance control so that there is no trace shift when the X10 button is depressed. Should the range of the front panel control be insufficient, it should be centralized and coarse correction made by R112. Complete the balance with the front panel control.
2. Set the invert balance pot R122 so that there is no trace shift when the invert button is depressed. When R122 is correctly set, there will be no trace shift when the variable gain control is operated.
3. Repeat steps (1) and (2) for CH2. Adjusting R212, coarse balance, and R222, invert balance, as required.
4. With CH1 and DC coupling selected, set the attenuator switch to 50mV/cm. Apply a 400mV pk-pk, 1kHz square wave from the calibrator. Adjust R135 for an 8cm pk-pk display. Apply the same signal to the CH2 input DC coupling and ground CH1. Set the CH2 attenuator switch to 50mV/cm. Select ADD CH2 on the CH1 function switches. Adjust R126 for an 8cm pk-pk trace. Reconnect signal to CH1 and DC couple. Depress INVert and de-select ADD CH2. Adjust R143 for an 8cm trace again.
5. Repeat for CH2 adjusting R235 for CH2 main gain, R226 for the cross channel gain and R243 for the invert gain.

NOTE: The order in which these adjustments are made is important and must be maintained.

5.3.7 ATTENUATOR COMPENSATION

The attenuator cover must be fitted.

1. Set CH1 attenuator to 20mV/cm and apply a 0.2V pk-pk, 1kHz square wave via a 1MΩ/28pF standardizer. Adjust C112 for a square corner to the display, operating the shift control to ensure that any over/under-shoot is not masked by the digital quantization. Repeat for CH2, adjusting C212.
2. Set CH1 attenuator to 0.2V/cm and apply a 1V, 1kHz square wave via the standardizer and adjust C108 for corner. Repeat for CH2, adjusting C206.
3. With CH1 attenuator still at 0.2V/cm, apply a 2V square wave via the standardizer and adjust C108 for a square corner. Repeat for CH2, adjusting C208.
4. Set CH1 attenuator to 2V/cm and apply a 10V square wave direct. Adjust C101 for a square corner. Repeat for CH2, adjusting C201.
5. With the CH1 attenuator still set to 2V/cm, apply a 20V square wave via the standardizer and adjust C103 for a square corner. Repeat for CH2, adjusting C203.
6. Set CH1 attenuator to 1mV/cm and select X10. Apply a 1mV square wave via the standardizer and adjust R16 for a square corner. Repeat for CH2, adjusting R26.
7. Remove the standardizer and check that all attenauator ranges give a square corner and are accurate to within ±2%.

5.3.8 INTERNAL CALIBRATOR

1. Set the frequency of the calibrator to 1kHz ±0.5% using R471 on the power supply board.
2. Using the D.V.M. set to a suitable d.c. voltage range, adjust the calibrator amplitude by R457 to give a reading of 0.5V ±5%.

5.3.9 OUTPUT UNIT

The calibration of the output unit is affected by the calibration of the main instrument and must therefore not be attempted until the latter is correct.

1. Select CONTINUOUS on the back panel PLOT MODE switch. If necessary push the front panel PLOT button to exit the plot mode. Select AUTO TRIGger, CH1 only with grounded input.

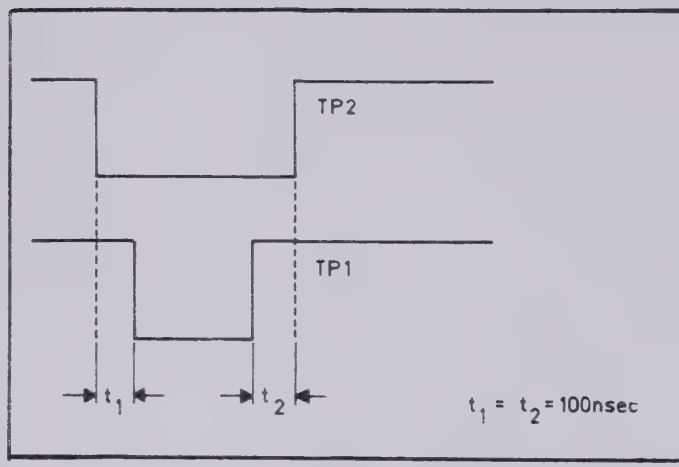


FIGURE 5-3 WRITE ENABLE TIMING WAVEFORMS

2. Connect a D.V.M. to the CH1 output BNC. Adjust the set zero preset, R805, for an output in the range 0 to +3mV.
3. Shift the trace fully off the top of the screen and press PLOT. Adjust the gain preset, R806, for an output of 427mV ± 1mV. Press PLOT and shift the trace fully off the bottom of the screen. Press PLOT again. Check that the output is in the range −423mV to −431mV. Exit the plot mode.
4. Connect the D.V.M. to the CH2 output and repeat steps 2 and 3, adjusting R827 and R828 respectively.

   Note: In single channel operation, both outputs display the same information and thus the CH1 output may again be used.
5. Connect the D.V.M. to the X output and adjust the set zero preset, R829, for an output of 0 ± 1mV.
6. Ground TP3 and adjust the gain preset, R830 to obtain +512mV ± 2mV.

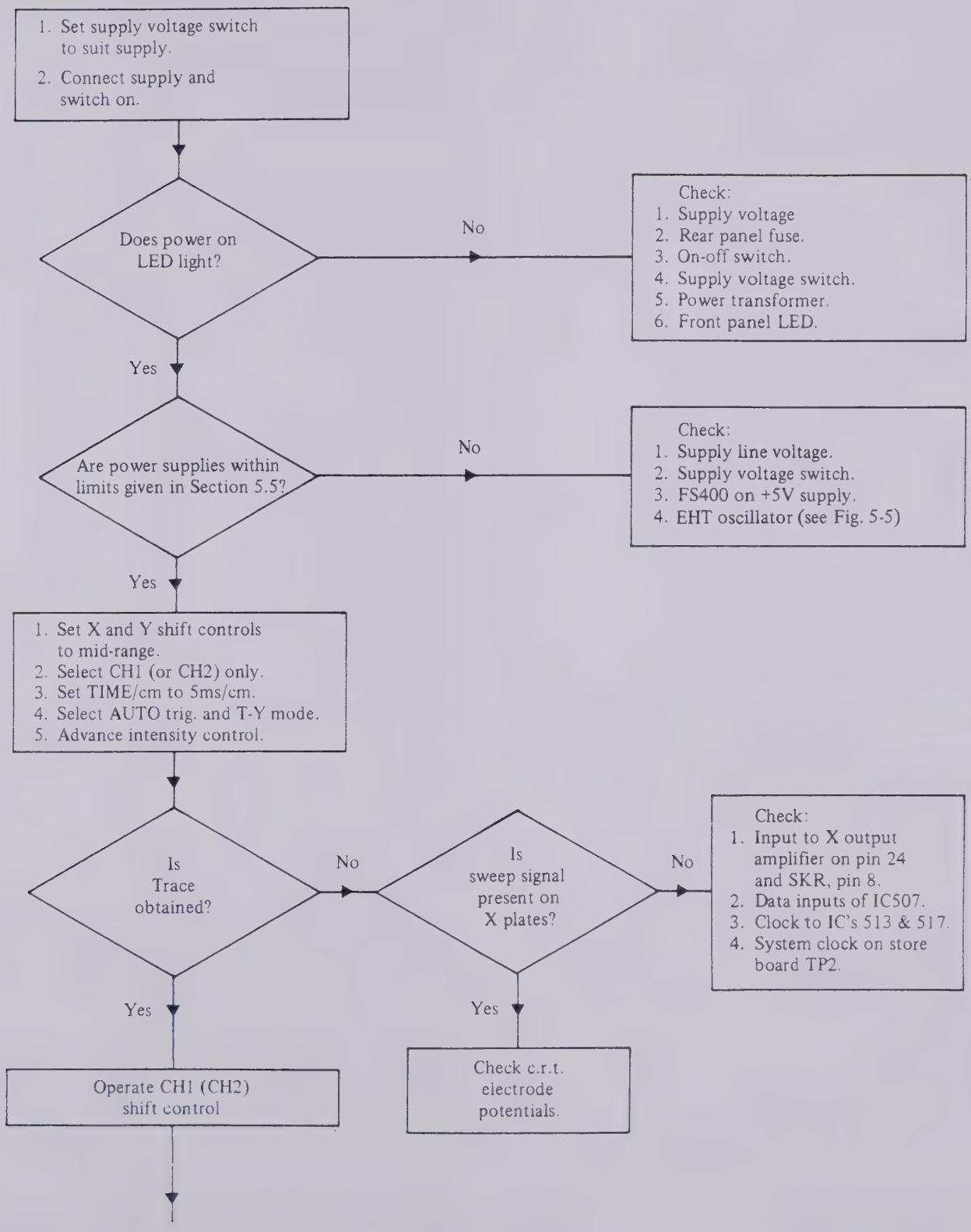
5.4 FAULT FINDING

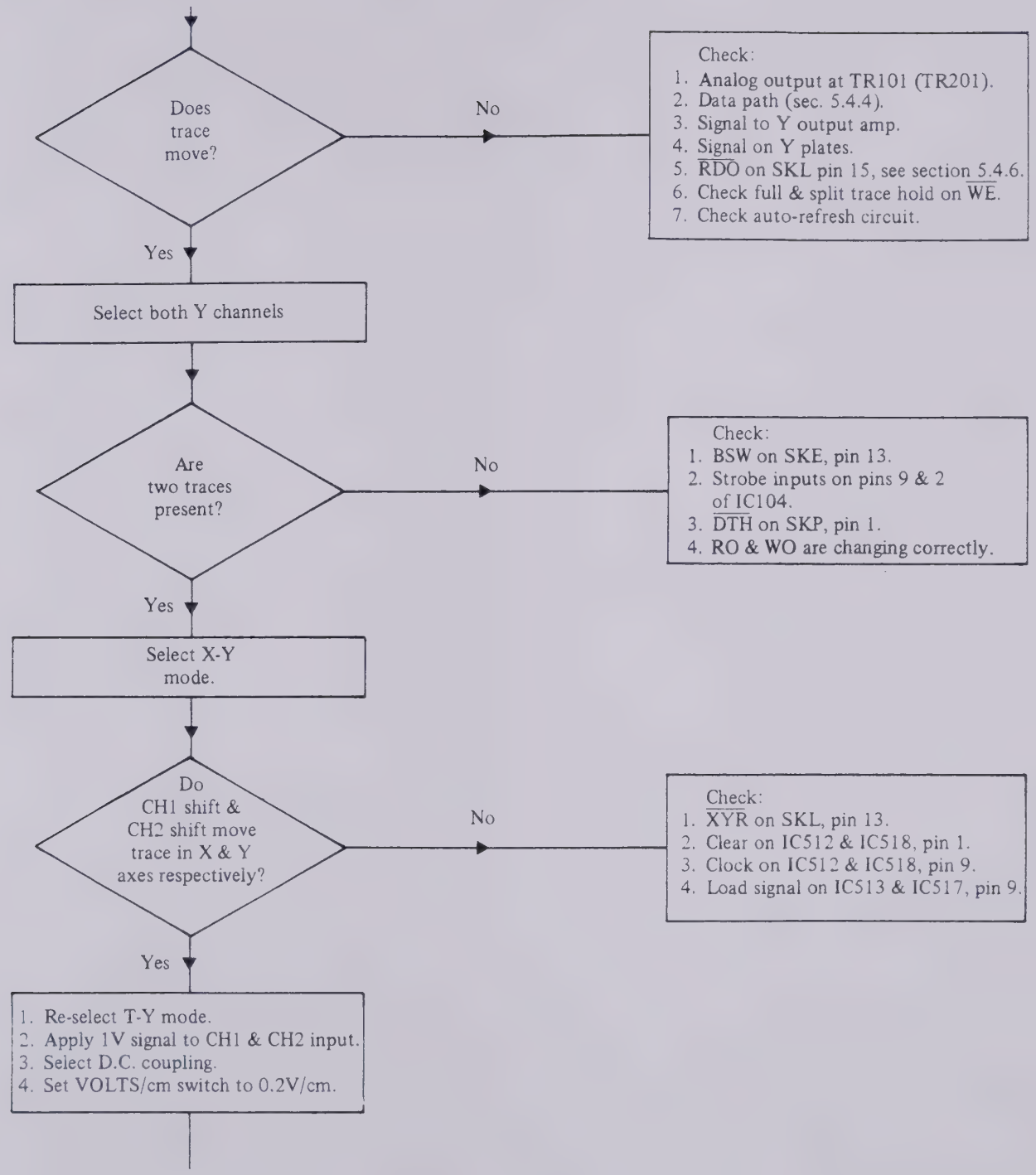
5.4.1 FAULT FINDING

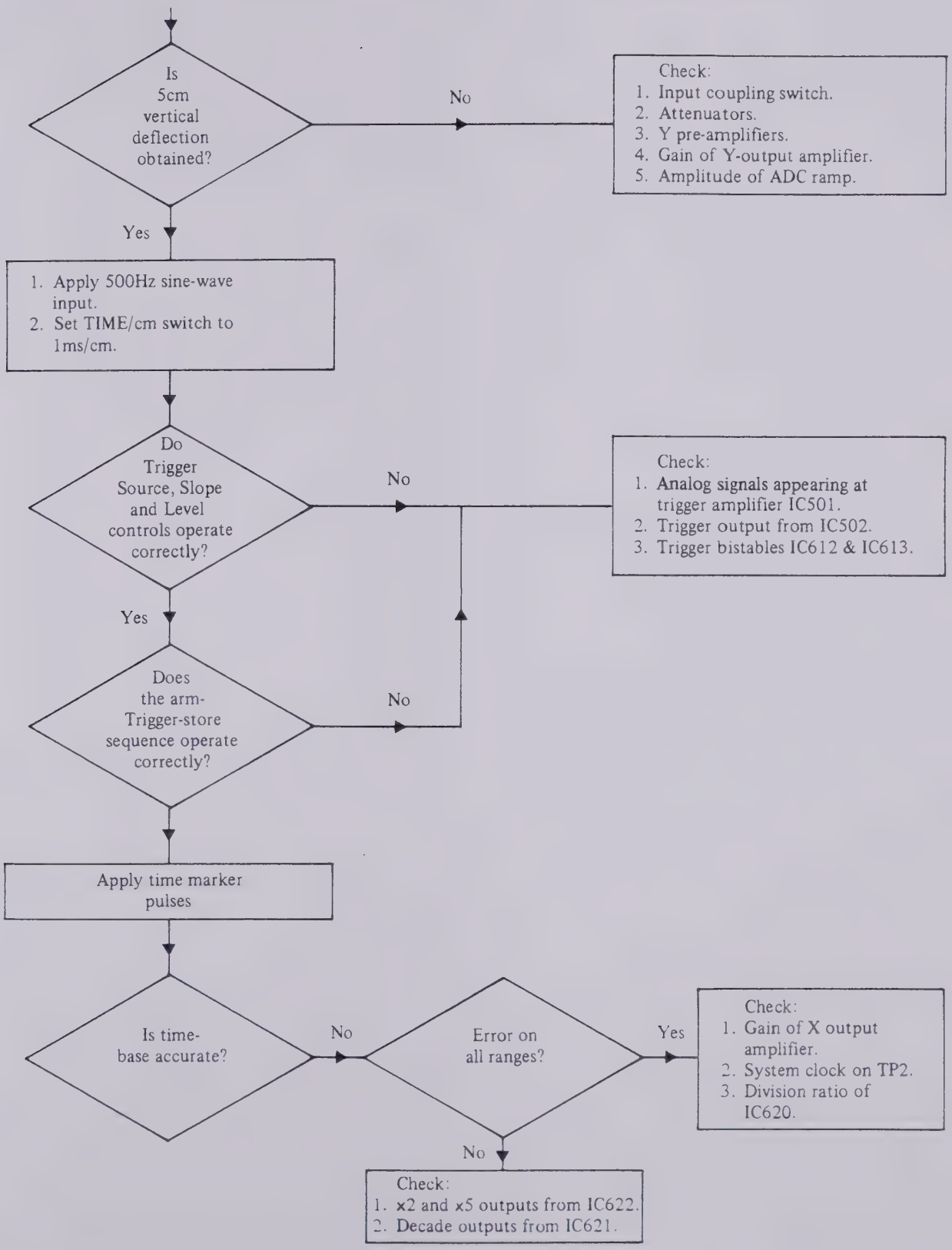
Faults may be attributed to specific areas of the instrument by following the fault location procedure in section 5.4.2. Faults in the data path, as opposed to analog or control logic faults, may be localised by following the flow chart of section 5.4.4. Note that detailed fault finding in the high frequency part of the ADC and clock chain will require a sampling oscilloscope or very high bandwidth read-time oscilloscope to resolve better than 3nsec.

More detailed analysis will be aided by the circuit voltages and waveforms shown in section 5.5.

5.4.2 FAULT LOCALIZATION


1. Set supply voltage switch to suit supply.
2. Connect supply and switch on.
Does power on LED light?
No
Check:
1. Supply voltage
2. Rear panel fuse.
3. On-off switch.
4. Supply voltage switch.
5. Power transformer.
6. Front panel LED.
Yes
Are power supplies within limits given in Section 5.5?
No
Check:
1. Supply line voltage.
2. Supply voltage switch.
3. FS400 on +5V supply.
4. EHT oscillator (see Fig. 5-5)
Yes
1. Set X and Y shift controls to mid-range.
2. Select CH1 (or CH2) only.
3. Set TIME/cm to 5ms/cm.
4. Select AUTO trig. and T-Y mode.
5. Advance intensity control.
Is Trace obtained?
No
Is sweep signal present on X plates?
No
Check:
1. Input to X output amplifier on pin 24 and SKR, pin 8.
2. Data inputs of IC507.
3. Clock to IC's 513 & 517.
4. System clock on store board TP2.
Yes
Yes
Operate CH1 (CH2) shift control
Check c.r.t. electrode potentials.


Does trace move?
No
Check:
1. Analog output at TR101 (TR201).
2. Data path (sec. 5.4.4).
3. Signal to Y output amp.
4. Signal on Y plates.
5. RDO on SKL pin 15, see section 5.4.6.
6. Check full & split trace hold on WE.
7. Check auto-refresh circuit.
Yes
Select both Y channels
Are two traces present?
No
Check:
1. BSW on SKE, pin 13.
2. Strobe inputs on pins 9 & 2 of IC104.
3. DTH on SKP, pin 1.
4. RO & WO are changing correctly.
Yes
Select X-Y mode.
Do CH1 shift & CH2 shift move trace in X & Y axes respectively?
No
Check:
1. XYR on SKL, pin 13.
2. Clear on IC512 & IC518, pin 1.
3. Clock on IC512 & IC518, pin 9.
4. Load signal on IC513 & IC517, pin 9.
Yes
1. Re-select T-Y mode.
2. Apply 1V signal to CH1 & CH2 input.
3. Select D.C. coupling.
4. Set VOLTS/cm switch to 0.2V/cm.


Is 5cm vertical deflection obtained?
No
Check:
1. Input coupling switch.
2. Attenuators.
3. Y pre-amplifiers.
4. Gain of Y-output amplifier.
5. Amplitude of ADC ramp.
Yes
1. Apply 500Hz sine-wave input.
2. Set TIME/cm switch to 1ms/cm.
Do Trigger Source, Slope and Level controls operate correctly?
No
Check:
1. Analog signals appearing at trigger amplifier IC501.
2. Trigger output from IC502.
3. Trigger bistables IC612 & IC613.
Yes
Does the arm-Trigger-store sequence operate correctly?
No
Apply time marker pulses
Is time-base accurate?
No
Error on all ranges?
Yes
Check:
1. Gain of X output amplifier.
2. System clock on TP2.
3. Division ratio of IC620.
No
Check:
1. x2 and x5 outputs from IC622.
2. Decade outputs from IC621.

5.4.3 DATA FAULTS

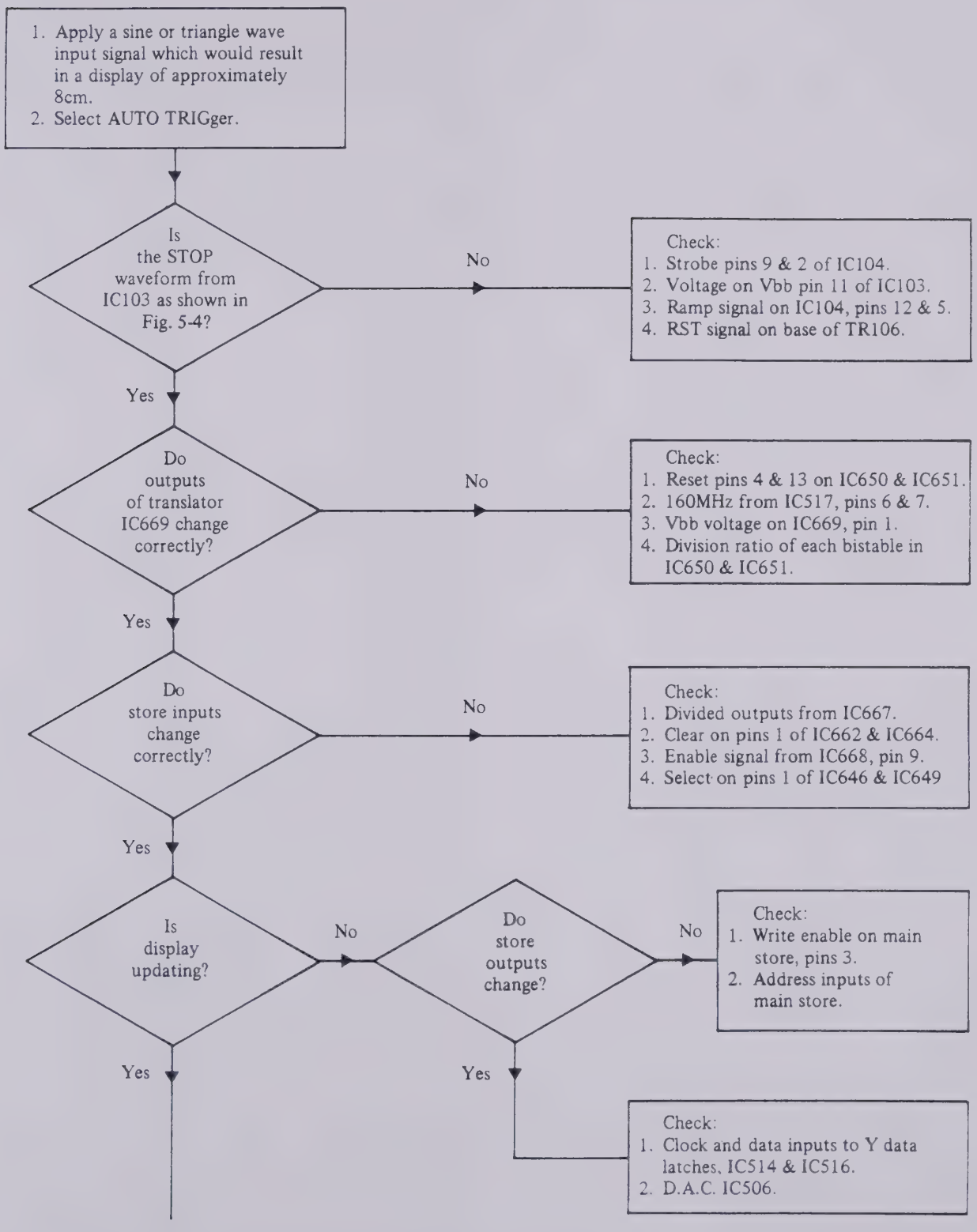
When tracing data faults which cause gross distortions (steps, discontinuities, etc.) of the display, it is helpful to distinguish between the following cases:

1. Addressing errors. These will occur at particular screen positions in the X direction regardless of the setting of the Y shift controls.
2. Data errors. These will occur at particular screen positions in the Y direction regardless of the setting of the Y shift controls.
3. Timing errors. These will usually be in the form of spikes or notches, generally random in nature, but often affected by the timebase and store controls.

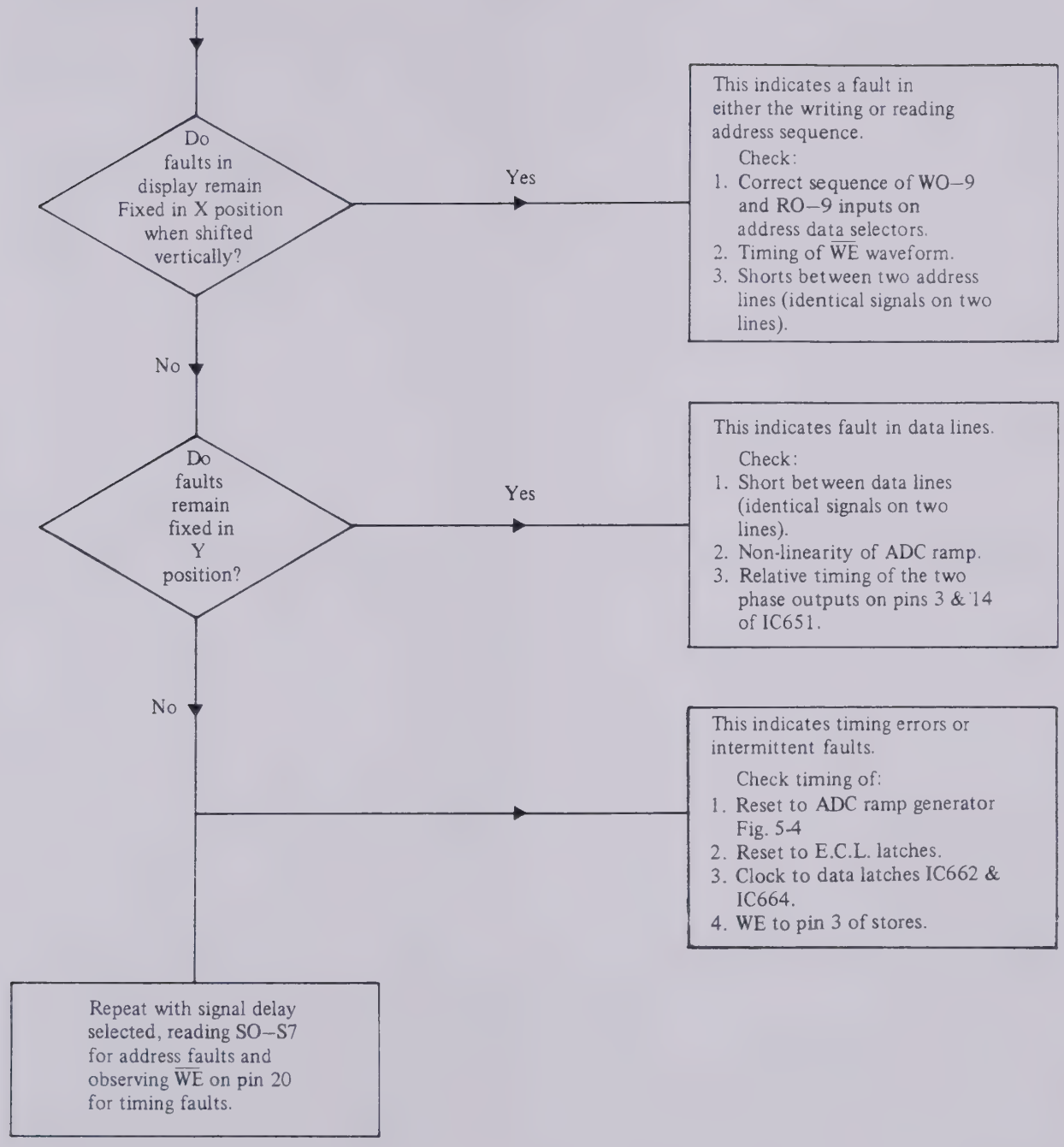
Addresses may be verified by looking for a true binary sequence. That is each bit changing at twice the frequency of the next most significant bit.

Fault finding on the data path will be simplified by using a ramp or triangle wave input as this will result approximately in a binary count, enabling the significance of each data line signal to be verified.

5.4.4 DATA PATH FAULT LOCALISATION


1. Apply a sine or triangle wave input signal which would result in a display of approximately 8cm.
2. Select AUTO TRIGger.
Is the STOP waveform from IC103 as shown in Fig. 5-4?
No
Check:
1. Strobe pins 9 & 2 of IC104.
2. Voltage on Vbb pin 11 of IC103.
3. Ramp signal on IC104, pins 12 & 5.
4. RST signal on base of TR106.
Yes
Do outputs of translator IC669 change correctly?
No
Check:
1. Reset pins 4 & 13 on IC650 & IC651.
2. 160MHz from IC517, pins 6 & 7.
3. Vbb voltage on IC669, pin 1.
4. Division ratio of each bistable in IC650 & IC651.
Yes
Do store inputs change correctly?
No
Check:
1. Divided outputs from IC667.
2. Clear on pins 1 of IC662 & IC664.
3. Enable signal from IC668, pin 9.
4. Select on pins 1 of IC646 & IC649
Yes
Is display updating?
No
Do store outputs change?
No
Check:
1. Write enable on main store, pins 3.
2. Address inputs of main store.
Yes
Yes
Check:
1. Clock and data inputs to Y data latches, IC514 & IC516.
2. D.A.C. IC506.

5.4.4 Continued


Do faults in display remain Fixed in X position when shifted vertically?
Yes
This indicates a fault in either the writing or reading address sequence.
Check:
1. Correct sequence of WO–9 and RO–9 inputs on address data selectors.
2. Timing of WE waveform.
3. Shorts between two address lines (identical signals on two lines).
No
Do faults remain fixed in Y position?
Yes
This indicates fault in data lines.
Check:
1. Short between data lines (identical signals on two lines).
2. Non-linearity of ADC ramp.
3. Relative timing of the two phase outputs on pins 3 & 14 of IC651.
No
This indicates timing errors or intermittent faults.
Check timing of:
1. Reset to ADC ramp generator Fig. 5-4
2. Reset to E.C.L. latches.
3. Clock to data latches IC662 & IC664.
4. WE to pin 3 of stores.
Repeat with signal delay selected, reading SO–S7 for address faults and observing WE on pin 20 for timing faults.

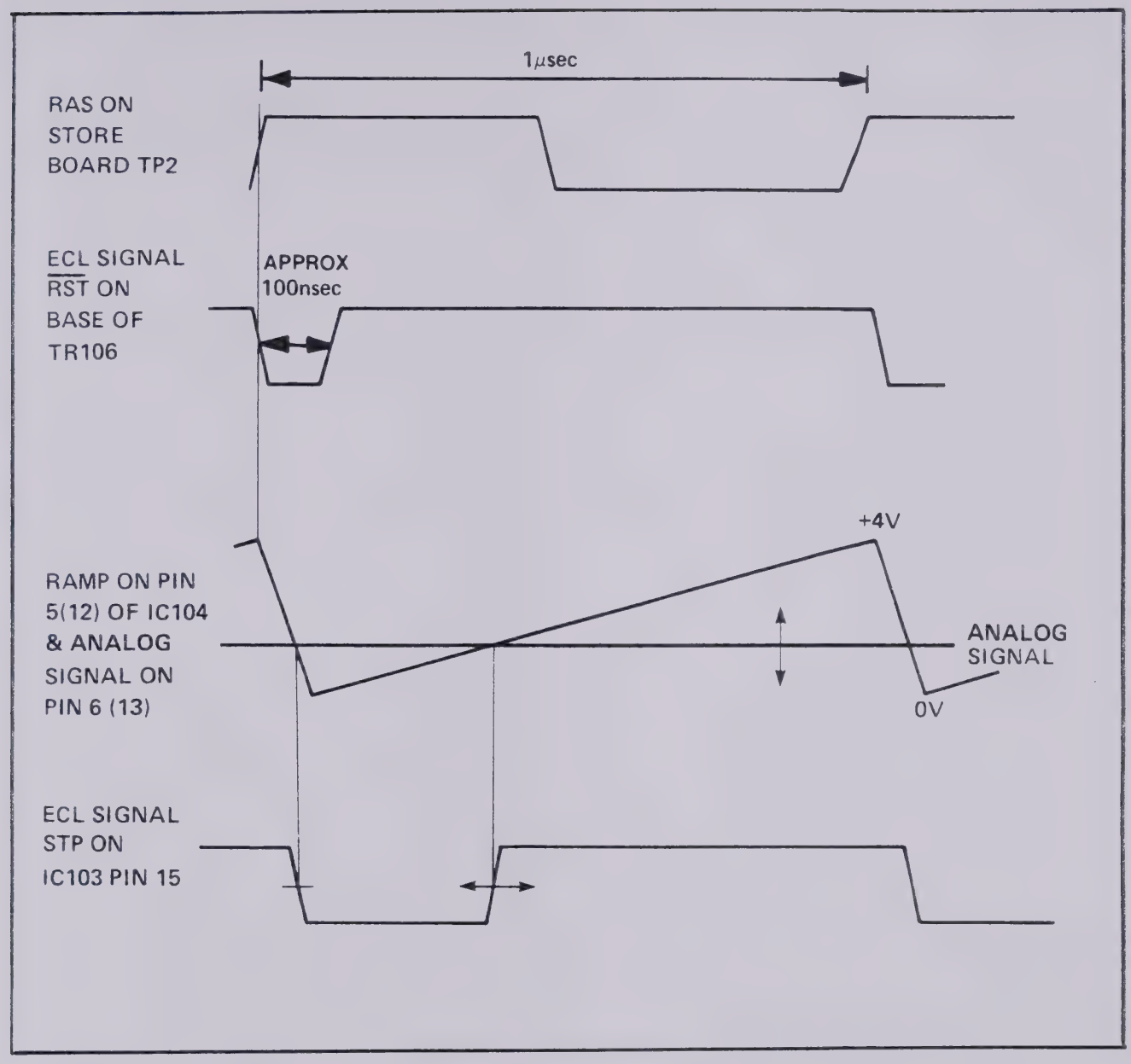
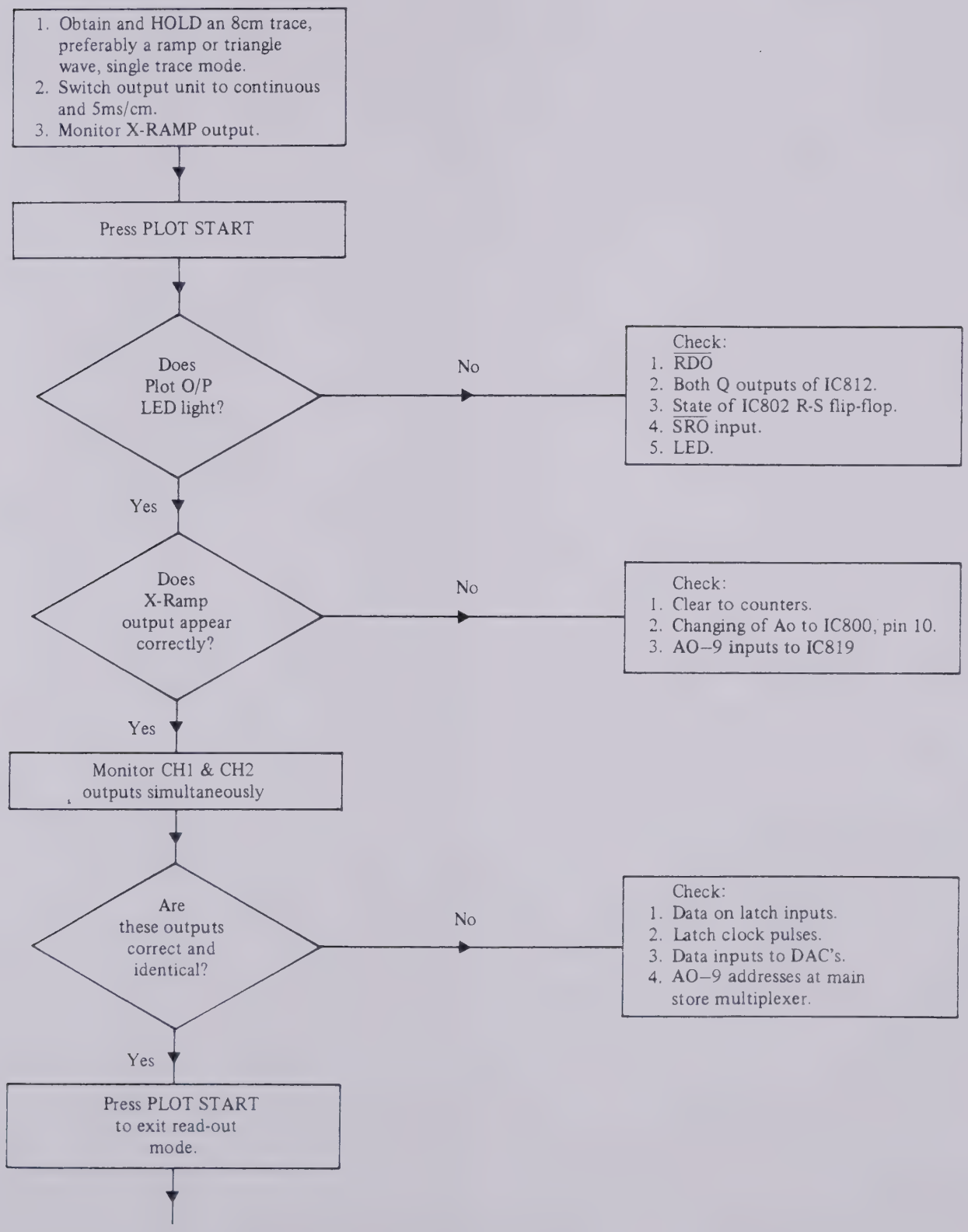
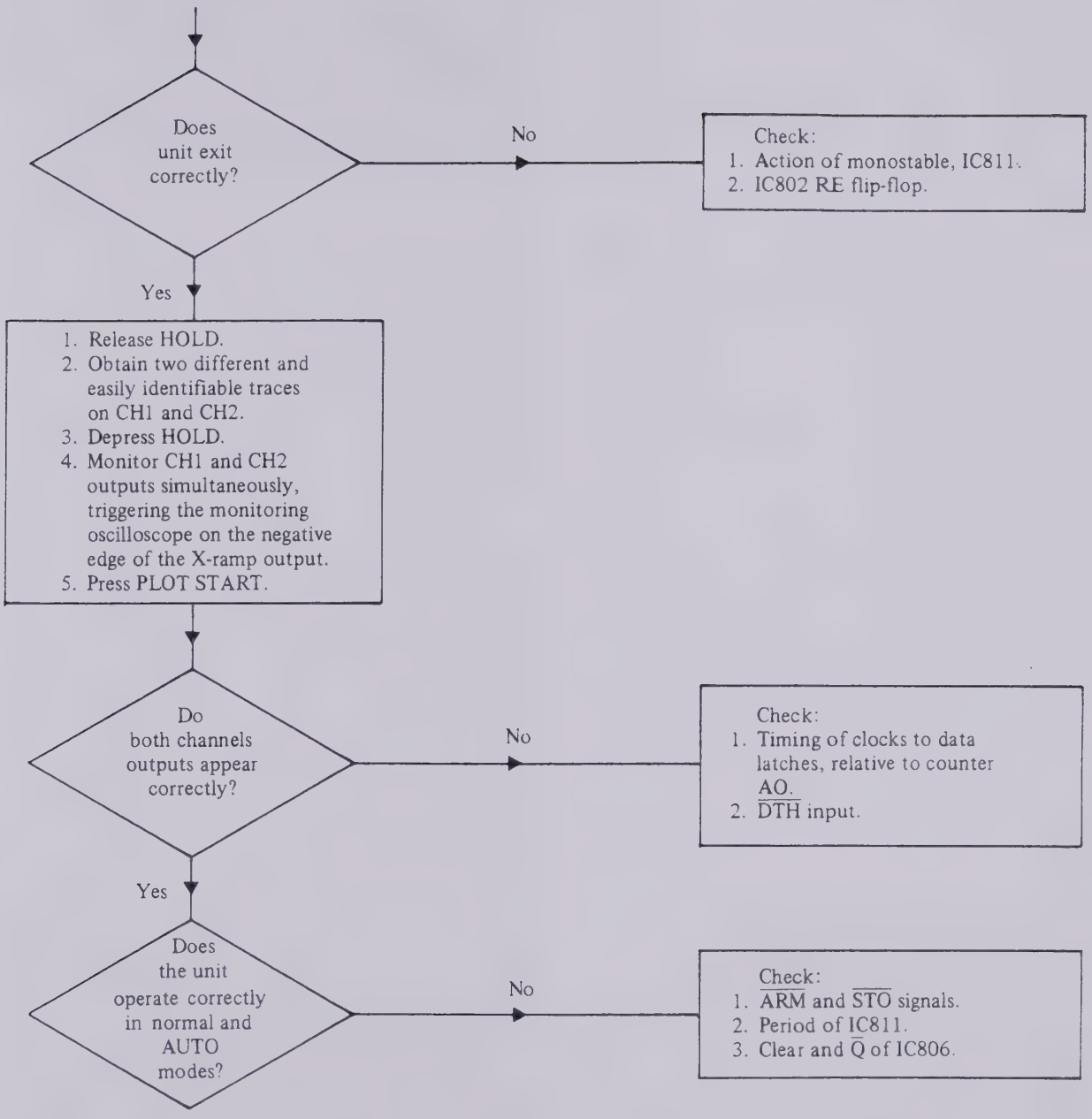

1μsec
RAS ON STORE BOARD TP2
ECL SIGNAL RST ON BASE OF TR106
APPROX 100nsec
+4V
RAMP ON PIN 5(12) OF IC104 & ANALOG SIGNAL ON PIN 6 (13)
ANALOG SIGNAL
0V
ECL SIGNAL STP ON IC103 PIN 15

FIGURE 5-4 ADC TIMING

5.4.5 OUTPUT UNIT FAULT LOCALISATION


1. Obtain and HOLD an 8cm trace, preferably a ramp or triangle wave, single trace mode.
2. Switch output unit to continuous and 5ms/cm.
3. Monitor X-RAMP output.
Press PLOT START
Does Plot O/P LED light?
No
Check:
1. RDO
2. Both Q outputs of IC812.
3. State of IC802 R-S flip-flop.
4. SRO input.
5. LED.
Yes
Does X-Ramp output appear correctly?
No
Check:
1. Clear to counters.
2. Changing of Ao to IC800, pin 10.
3. AO–9 inputs to IC819
Yes
Monitor CH1 & CH2 outputs simultaneously
Are these outputs correct and identical?
No
Check:
1. Data on latch inputs.
2. Latch clock pulses.
3. Data inputs to DAC's.
4. AO–9 addresses at main store multiplexer.
Yes
Press PLOT START to exit read-out mode.


Does unit exit correctly?
No
Check:
1. Action of monostable, IC811.
2. IC802 RE flip-flop.
Yes
1. Release HOLD.
2. Obtain two different and easily identifiable traces on CH1 and CH2.
3. Depress HOLD.
4. Monitor CH1 and CH2 outputs simultaneously, triggering the monitoring oscilloscope on the negative edge of the X-ramp output.
5. Press PLOT START.
Do both channels outputs appear correctly?
No
Check:
1. Timing of clocks to data latches, relative to counter AO.
2. $\overline{DTH}$ input.
Yes
Does the unit operate correctly in normal and AUTO modes?
No
Check:
1. $\overline{ARM}$ and $\overline{STO}$ signals.
2. Period of IC811.
3. Clear and $\overline{Q}$ of IC806.

5.5 CIRCUIT VOLTAGES

The following voltages may be used as a general guide during faultfinding. All voltages are measured with respect to ground (chassis) with a high impedance instrument with the supply line voltage at the nominal value set on the SUPPLY VOLTAGE switch. Voltages marked (*) are dependent upon front panel control settings and must be interpreted accordingly. The readings are taken with the front panel controls set as follows unless otherwise indicated:-

Both Y SHIFT controls centralized.

CH1 and CH2 inputs switched to GND.

CH1 and CH2 selected with no other signal functions.

DISPLAY MODE to X-Y.

TRIGger SOURCE to CH1 and AUTO TRIGger.

TIME/cm to 10ms/cm.

TRIGger LEVEL to mid range.

TRIGger WINDOW to mid range.

TRIGger SLOPE to dual slope.

Y AMPLIFIER BOARD

1.	IC100/IC200 pin 6*		≪±1mV
2.	IC101/IC201 pin 6		<±1mV
3.	IC102/IC202 pin 6*		2.4V
4.	TR101 emitter*		1.7V
5.	TR100 base*		10.5V
6.	TR102 emitter	w.r.t.	6.2V
7.	TR103 emitter	+12V	6.2V
8.	TR10/TR20 collector*		0.83V
9.	IC103 pin 11		1.25V
10.	TR107 base		1.25V

STORE BOARD

1.	TR602 base	−4.9V
2.	IC669 pin 1	−1.25V

DISPLAY BOARD

IC507 pin 2 IC506 pin 6	+ 2.5V
IC508 pins 14 & 15	0V NOM
IC501 pin 6*	0V
TR501 emitter*	0V
IC504 pin 6*	0V
IC503 pin 6* (X-Y)	0V

POWER SUPPLY BOARD

	Min	Max
pin 32 with respect to pin 34	4.75V	5.25V
pin 38 with respect to pin 36	−4.75V	−5.25V
pin 26 with respect to pin 27	11.4V	12.6V
pin 29 with respect to pin 27	−11.4V	−12.6V

C428 "+" terminal Typ	+17.5V
Typical ripple	0.5V p-p
C429 "+" terminal Typ	+5.5V
Typical ripple	0.5V p-p
C430 "+" terminal Typ	+10.5V
Typical ripple	0.7V p-p
C431 "+" terminal Typ	+5.5V
Typical ripple	0.5V p-p
TR403 base	0V
TR410 base w.r.t. +12V	−5.7V
TR415, TR418 TR408, TR412 } base	+10.5V
TR414, TR417 collector (Use CH1 Y shift, if necessary to equalize voltages.)	+103V
TR407, TR411 collector (Use CH2 Y shift, if necessary, to equalize voltages.)	+103V

LOGIC LEVELS

TTL Inputs:	Logic '0' max	+0.8V
	Logic '1' min	+2.0V
Outputs:	Logic '0' max	+0.4V
	Logic '1' min	+2.4V
Typical Levels:	Logic '0'	+0.2V
	Logic '1'	+4.0V
ECL Inputs:	Logic '0' max	−1.5V
	Logic '1' min	−1.2V
Outputs:	Logic '0' max	−1.68V
	Logic '1' min	−1.08V
Typical Levels:	Logic '0'	−1.75V
	Logic '1'	−0.9V

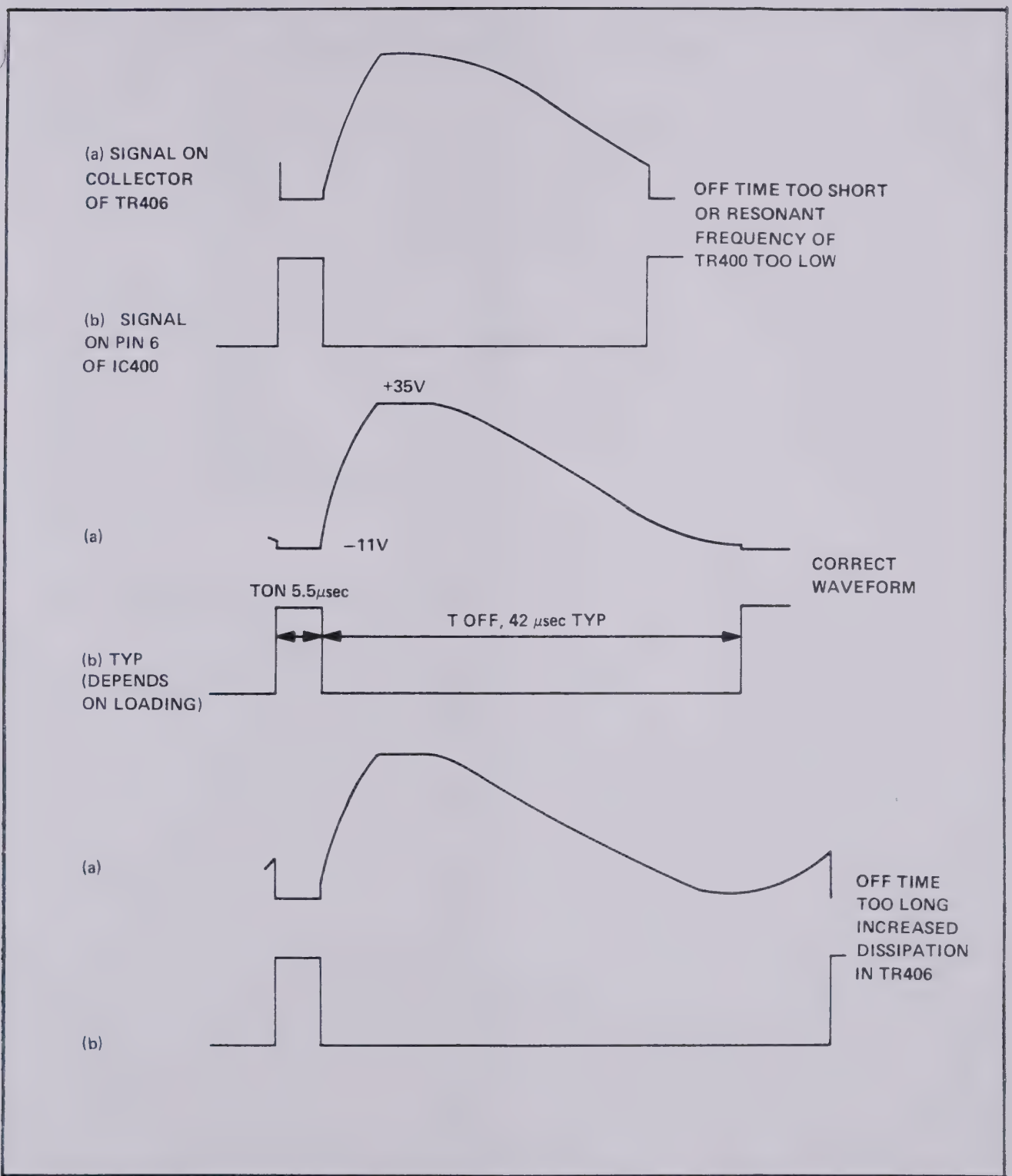


FIGURE 5-5 EHT OSCILLATOR WAVEFORMS

6.1 ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	1/2 W	10%	unless otherwise stated
CF	Carbon Film	1/8 W	5%	unless otherwise stated
MO	Metal Oxide	1/2 W	2%	unless otherwise stated
MF	Metal Film	1/4 W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potentiometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+ 80% - 25%	
CE(2)	Ceramic	500V	± 10%	unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		± 10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		± 10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (aluminium)		+ 50% - 10%	
T	Tantalum		+ 50% - 10%	

6.2 PARTS ORDERING INSTRUCTIONS

a. When ordering parts add:

1. "AD-2" before all 5 digit part numbers.
   Example: Part number 21806 becomes AD-221806.

2. "AD-20" before all 4 digit part numbers.

3. "AD-2" and remove "alpha-numeric/" prefix from 5 digit number
   Example: Part number A4/39314 becomes AD-239314.

OS4100 'Y' AMPLIFIER

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R100	4k7	CP		A4/39314
R101	100k	CP		A4/39315
R102	10k1	MF	0.5	37778
R103	111k	MF	0.5	37779
R104				
R105	1M	MF		26346
R106	68k	CF		21816
R107	68k	CF		21816
R108	1k	CF		21799
R109	470	CF		21797
R110	470k	CC	5	4906
R111				
R112	10k	PCP		39228
R113	10k	CF		21809
R114	10k	CF		21809
R115				
R116	3k3	CF		21803
R117	100	CF		21794
R118	3k3	CF		21803
R119	15k	CF		28727
R120	100	CF		21794
R121				
R122	20k	PCP		39229
R123	2k7	CF	2	38604
R124	12k	MF	2	38620
R125				
R126	500	PCP		39232
R127	2k2	CF		21802
R128	2k7	CF		28726
R129	.82k	CF		21818
R130	15k	CF		28727
R131	3k3	CF		21803
R132	1k2	CF		21800
R133				
R134	2k2	CF		21802
R135	500	PCP		39232
R136	2k2	CF		21802
R137	9k1	MF	2	38617
R138	5k6	CF		21806
R142	1k2	CF		21800
R143	500	PCP		39232
R144	680	CF		28723
R145	1k	CF		21799
R146	2k2	CF		21802
R147	5k6	CF		21806
R148	330	CF		28721
R149				
R150	6k3	MF	2	38613
R151	5k6	CF		21806
R152	170	CF		28720
R153				
R154	4k7	CF		21805
R155	4k7	CF		21805
R156	100	CF		21794
R157	100	CF		21794
R158	1k8	CF		28725

Ref	Value	Description	Tol % ±	Part No
R161	5k6	CF		21806
R164	100	CF		21794
R165	150	CF		28719
R166	150	CF		28719
R167	560	CF		21798
R168	3k9	CF		21804
R169	2k7	CF		28726
R170	82	CF		28717
R171	82	CF		28717
R200	4k7	CP		A4/39314
R201	100k	CP		A4/39315
R202	10k1	MF	0.5	37778
R203	111k	MF	0.5	37779
R204				
R205	1M	MF		26346
R206	68k	CF		21816
R207	68k	CF		21816
R208	1k	CF		21799
R209	470	CF		21797
R210	470k	CC	5	4906
R211				
R212	10k	PCP		39228
R213	10k	CF		21809
R214	10k	CF		21809
R215				
R216	3k3	CF		21803
R217	100	CF		21794
R218	3k3	CF		21803
R219	15k	CF		28727
R220	100	CF		21794
R221				
R222	20k	PCP		39229
R223	2k7	MF	2	38604
R224	12k	MF	2	38620
R225				
R226	500	PCP		39232
R227	2k2	CF		21802
R228	2k7	CF		28726
R229	82k	CF		21818
R230	15k	CF		28727
R231	3k3	CF		21803
R232	1k2	CF		21800
R233				
R234	2k2	CF		21802
R235	500	PCP		39232
R236	2k2	CF		21802
R237	9k1	CF		38617
R238	5k6	CF		21806
R242	1k2	CF		21800
R243	500	PCP		39232
R244	680	CF		28723
R245	1k	CF		21799
R246	2k2	CF		21802
R247	5k6	CF		21806
R248	330	CF		28721
R258	1k8	CF	5	28725

OS4100 'Y' AMPLIFIER (Cont.)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS				
C100	470pF	PS		35916
C101	0/6pF	TRIMMER		29421
C102	12pF	CE(2)		22365
C103	0/6pF	TRIMMER		29421
C104				
C105	15pF	CE(2)		22366
C106	0/6pF	TRIMMER		29421
C107	12pF	CE(2)		22365
C108	0/6pF	TRIMMER		29421
C109	33pF	CE(2)		22370
C112	0/6pF	TRIMMER		29421
C113	.01μF	CE(2)		24902
C114				
C115	47μF	T	16V	39215
C116	47μF	T	16V	39215
C117				
C118	1000pF	CE(2)		22387
C119				
C120	33μF	E	16V	32173
C121	33μF	E	16V	32173
C122	0.1μF	CE(2)		37018
C123	180pF	CE(2)		33898
C124	0.1μF	CE(2)		37018
C125	33μF	E	16V	32173
C126	33μF	E	16V	32173
C127	0.1μF	CE(2)		37018
C130	.01μF	CE(2)	250V	22395
C131	.01μF	CE(2)	250V	22395
C132	.01μF	CE(2)	250V	22395
C133	.01μF	CE(2)	250V	22395
C134				
C135	220pF	PS		35914
C136	.01μF	CE(2)		37018
C137				
C138	8.2pF	CE(2)		22363
C200	470pF	PS		35916
C201				
C202	12pF	CE(2)		22365
C205	15pF	CE(2)		22366
C206				
C207	12pF	CE(2)		22365
C208				
C209	33pF	CE(2)		22370
C213	.01μF	CE(2)		24902
C214				
C215	47μF	T	16V	39215
C216	47μF	T	16V	39215
C217				
C218	1000pF	CE(2)		22387
C219				
C220	33μF	E	16V	32173
C221	33μF	E	16V	32173
C222	0.1μF	CE(2)		37018
C223	180pF	CE(2)		33898

Ref	Value	Description	Tol % ±	Part No
TRANSISTORS				
TR100		BC212		29327
TR101		BC182		33205
TR102		MPS3640		39323
TR103		MPS3640		39323
TR104		BC212		29327
TR105		BC212		29327
TR106		2N2369		23307
TR107		2N2369		23307
TR200		BC212		29327
TR201		BC182		33205
DIODES				
D100		PAD5		40839
D101		PAD5		40839
D102	5V1	ZENER		33928
D103	5V1	ZENER		33928
D104	8V2	ZENER		33933
D105		1N4148		23802
D106		1N4148		23802
D107	6V2	ZENER		40045
D108				
D109		1N4148		23802
D200		PAD5		40839
D201		PAD5		40839
D202	5V1	ZENER		33928
D203	5V1	ZENER		33928
D204	8V2	ZENER		33933
D205		1N4148		23802
D206		1N4148		23802
INTEGRATED CIRCUITS				
IC100		LF357B		40811
IC101		LF357B		40811
IC102		LF357B		40811
IC103				
IC104		MC1414		36928
IC105		74LS00		36730
IC200		LF357B		40811
IC201		LF357B		40811
IC202		LF357B		40811
SWITCHES				
S100				A3/39304
S101				A3/39304
S102				A3/39304
S103				A3/39304
S104				A3/39303
S200				A3/39304
S201				A3/39304
S202				A3/39304
S203				A3/39304
S204				A3/39303
MISCELLANEOUS				
L100	2.7μH			37801

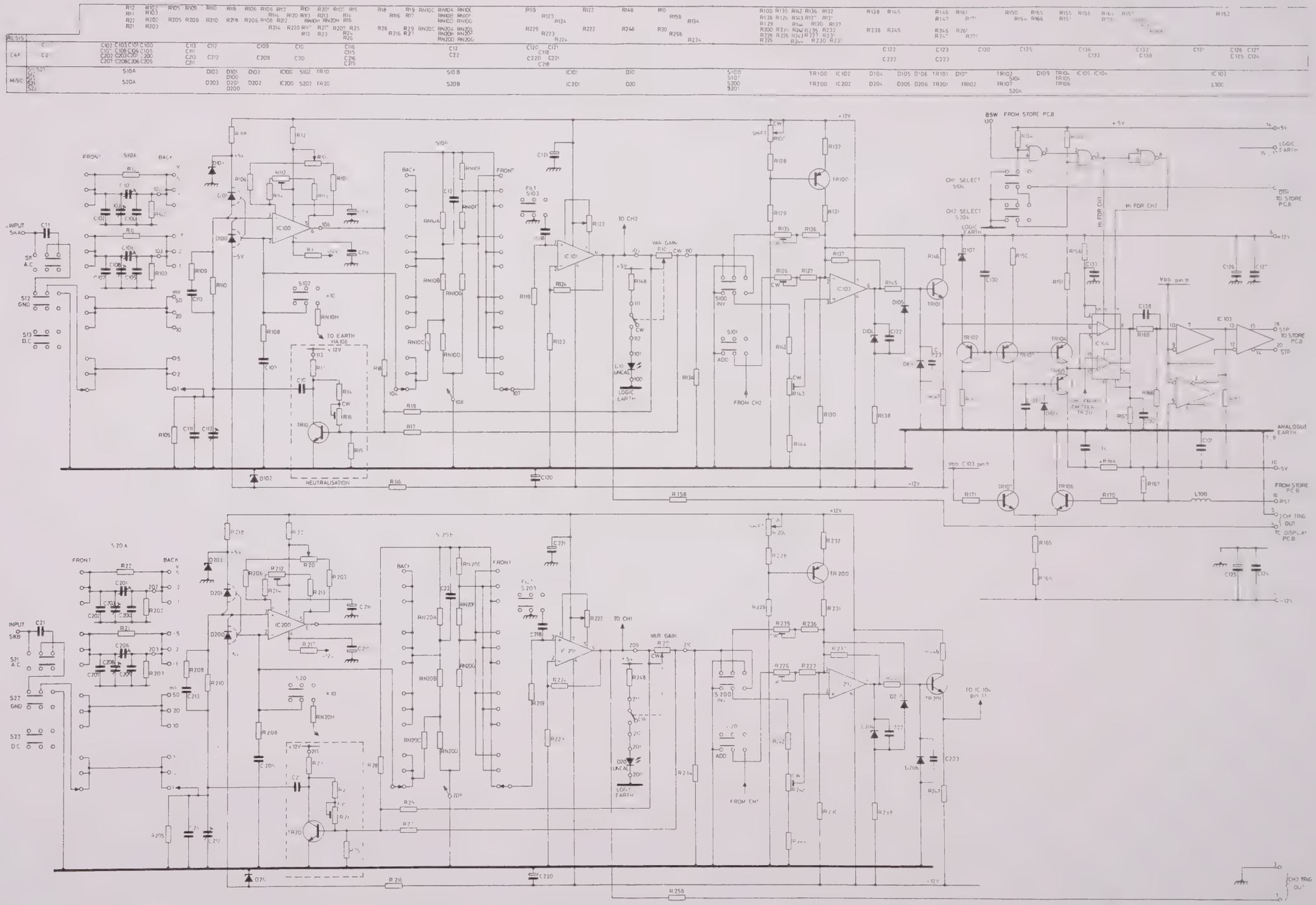


FIGURE 6-1 'Y' AMPLIFIER CIRCUIT DIAGRAM

OS4100 LOGIC P.C.B.

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R601	4k7 x 8	RESISTOR NETWORK		39225
R602	330	CF		28721
R603	4k7 x 8	RESISTOR NETWORK		39225
R604	330	CF		28721
R605	330	CF		28721
R606	39k	CF		28728
R607	4k7	CF		21805
R608	10k	PCP		39265
R609	10k	PCP		39265
R610	330	CF		28721
R611	100	CF		21794
R612	330	CF		28721
R613	390	CF		28722
R614	560	CF		21798
R615	560 x 8	RESISTOR NETWORK		39258
R616	560 x 8	RESISTOR NETWORK		39258
R617	560 x 8	RESISTOR NETWORK		39258
R618	560 x 8	RESISTOR NETWORK		39258
R619	560 x 8	RESISTOR NETWORK		39258
R620	1k5	CF		21801
R621	680	CF		28723
R622	3k9	CF		21804
R623	2k7	CF		28726
R624	220	CF A.O.T.		21796
R625	100	CF		21794
R626	1k5	CF		21801
R627	1k			39233
CAPACITORS				
C601	10µF	E	25V	32180
C602	.01µF	CE(2)	250V	22395
C603	.01µF	CE(2)	250V	22395
C604	.01µF	CE(2)	250V	22395
C605	.01µF	CE(2)	250V	22395
C606	100pF	CE(2)		22376
C607	100pF	CE(2)		22376
C608	.01µF	CE(2)	250V	22395
C609	.01µF	CE(2)	250V	22395
C610	.01µF	CE(2)	250V	22395
C611	.01µF	CE(2)	250V	22395
C612	47µF	T	16V	39215
C613				
C614	.01µF	CE(2)	250V	22395
C615	.01µF	CE(2)	250V	22395
C616	.01µF	CE(2)	250V	22395
C617	.01µF	CE(2)	250V	22395
C618	47µF	T	16V	39215
C619				
C620	.01µF	CE(2)	250V	22395
C621				
C622	1500pF	CE(2)		22388
C623	18pF	CE(2)		22367
C624	1500pF	CE(2)		22388
C625	2.7pF	CE(2)		36599
C626	10pF	CE(2) A.O.T.		22364
C627	18pF	CE(2)		22367
C628	1500pF	CE(2)		22388
C629	100pF	CE(2)		22376
C630	8.2pF	CE(2)		22363
C631				
C632	1500pF	CE(2)		22388
C633	1500pF	CE(2)		22388
C634	1500pF	CE(2)		22388
C635	82pF	CE(2)		22375
C636	4.7µF	T	35V	53249
C637	1500pF	CE(2)		22388
C638	1500pF	CE(2)		22388
C639	.01µF	CE(2)	250V	22395
C640	.01µF	CE(2)	250V	22395
C641	.01µF	CE(2)	250V	22395
C642	5.6pF	CE(2)		22361
C643	4.7pF	CE(2)		29649
C644	.01µF	CE(2)	250V	22395
C645				
C646	10pF	CE(2)		22364
DIODES				
D601		OA47		4468
D602		OA47		4468
D603		OA47		4468
D604		1N4148		23802
D605	5V6	ZENER		33929
INTEGRATED CIRCUITS				
IC601		74LS157		36735
IC602		74LS112		36468
IC603		74LS00		36730
IC604		74LS175		36728
IC605		74LS175		36728
IC606		74LS00		36730
IC607		74LS156		39237
IC608		74LS122		39238
IC609		74LS112		36468
IC610		74LS00		36730
IC611		74LS20		39236
IC612		74LS112		36468
IC613		74LS74		36732
IC614		74LS10		36867
IC615		74LS153		36247
IC616		74LS175		36728
IC617		74LS20		39236
IC618		74LS221		39239
IC619				
IC620		74LS290		39240
IC621		MK5009		34952
IC622		74LS153		36247
IC623		74LS293		39241
IC624		74LS293		39241
IC625		74LS293		39241
IC626		74LS293		39241

OS4100 LOGIC P.C.B. (Cont.)

Ref	Value	Description	Tol % ±	Part No
INTEGRATED CIRCUITS (Cont.)				
IC627		74LS112		36468
IC628		74LS293		39241
IC629		74LS112		36468
IC630		73LD153		36247
IC631				
IC632		74LS153		36247
IC633		74LS153		36247
IC634				
IC635		74LS153		36247
IC636				
IC637		74LS153		36247
IC638		2012L		39248
IC639		2012L		39248
IC640		2012L		39248
IC641		2012L		39248
IC642		2012L		39248
IC643		2012L		39248
IC644		2012L		39248
IC645		2012L		39248
IC646		74LS157		36735
IC647		74LS175		36728
IC648		74LS175		36728
IC649		74LS157		36735
IC650		10131		39246
IC651		10231		39247
IC652		10231		39247
IC653		2101-1		39249
IC654		74LS293		39241
IC655		74LS293		39241
IC656		2101-1		39249
IC657		10216		39903
IC658		10102		39243
IC659		10231		39247
IC660		74121		52099
IC661		74LS86		38916
IC662		74LS175		36728
IC663		74LS04		36731
IC664		74LS175		36728
IC665		74LS290		39240
IC666		74LS00		36730
IC667		79LS293		39241
IC668		74LS112		36468
IC669		10125		39245
MISCELLANEOUS				
L601	0.47μH			33336
L602	0.47μH			33336
L603				A4/39885
TR601		2N2369		23307
TR602		BF371		36275

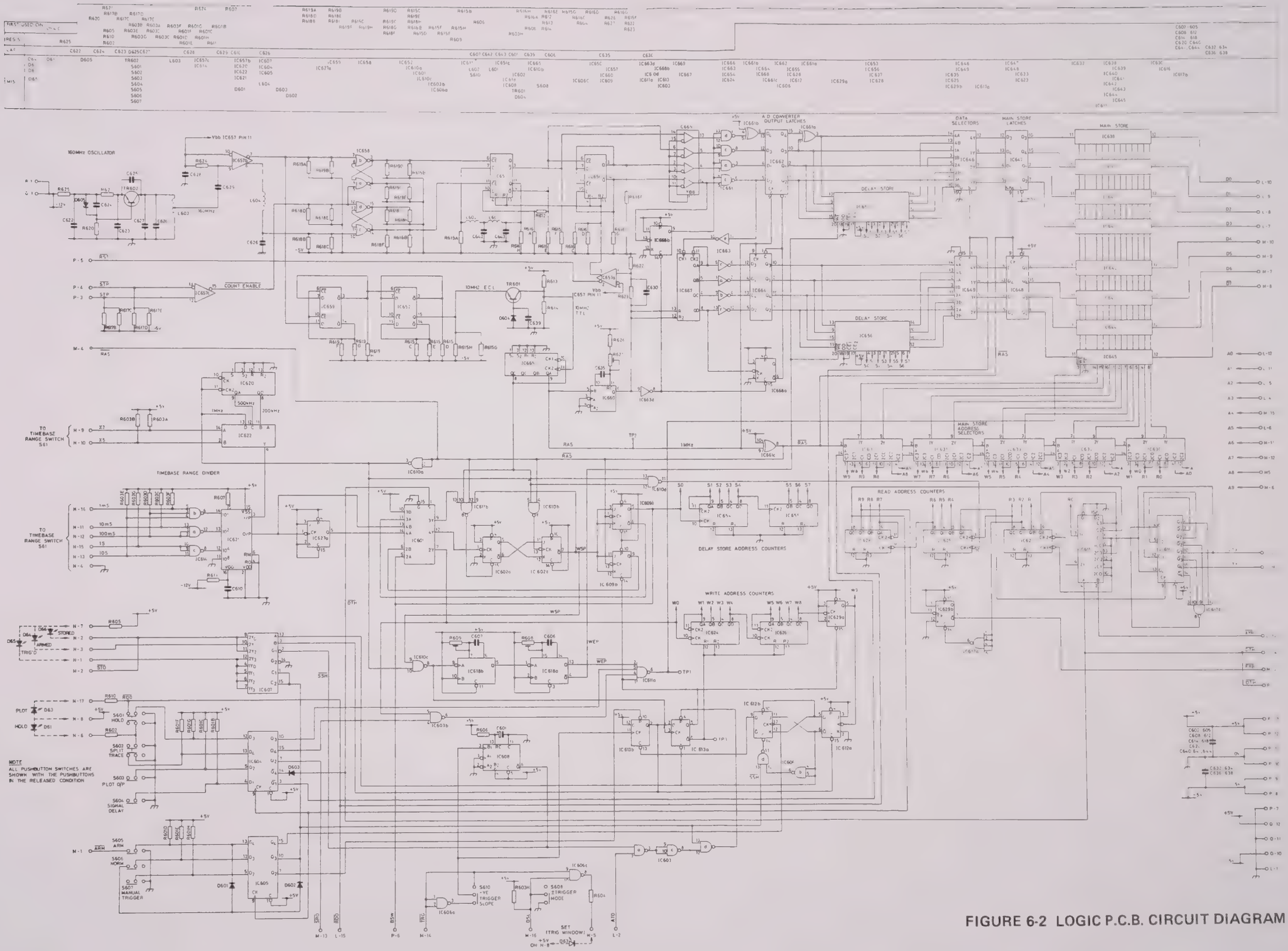


FIGURE 6-2 LOGIC P.C.B. CIRCUIT DIAGRAM

OS4100 DISPLAY P.C.B.

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R501	10k	CP		39228
R502	8k2	CF		21808
R503	1k	CF		21799
R504	12k	CF		21810
R505	220	CF		21796
R506	1M	CF		31840
R507	220k	CF		31823
R508	220	CF		21796
R509	12k	CF		21810
R510	1k	CF		21799
R511	1k	CF		21799
R512	1k	CF		21799
R513	111k	MF	0.5	37779
R514	3k9	CF		21804
R515				
R516	900k	MF	0.5	31929
R517	56k	CF		28729
R518	15k	CF		28727
R519	10k	CF		21809
R520	10k	CF		21809
R521	75k	MF	2	38639
R522	3k9	CF		21804
R523	1k	CF		21799
R524	10k	CF		21809
R525	560	CF		21798
R526	470	CF		21797
R527	470	CF		21797
R528	10k	CF		21809
R529	560	CF		21798
R530				
R531	100	CF		21819
R532	100k	CF		21819
R533	22	CF		28710
R534				
R535	68k	CF		21816
R536	390	CF		28722
R537	22	CF		28710
R538	22	CF		28710
R539	560	CF		21798
R540	500	MF	0.5	39223
R541	100	MF	0.5	39224
R542	390	CF		28722
R543	1k	CF		21799
R544	1k	CF		21799
R545	390	CF		28722
R546	5k6	CF		21806
R547	100k	CF		21819
R548	3k9	CF		21804
R549	500	MF	0.5	39223
R550	560	CF		21798
R551	1k2	CF		21800
R552	1k8	CF		28725
R553	1k8	CF		28725
R554	1k2	MF	2	38596
R555	2k	PCP		40178
R556	2k	PCP		40178
R557	1k2	CF		21800
R558	4k7 x 8	RESISTOR MODULE		39225
R559				
R560	2k7	CF		28726
R561	2k7	CF		28726
R562				
R563	100k	CF		21819
R564				
R565	1k	CF		21799
R566	22	CF		28710
CAPACITORS				
C501				
C502	3300pF	PS	2½ 63V	35921
C503	1000pF	PS	2½ 63V	35918
C504	3300pF	PS	2½ 63V	35921
C505	1000pF	PS	2½ 63V	35918
C506	.047µF	CE(2)	10V	19657
C507	100pF	CE(2)		22376
C508		CE(2)	100V	37018
C509		CE(2)	100V	37018
C510	470pF	CE(2)		22383
C511		PF	100V	37018
C512		PF	100V	37018
C513	220pF	PS	2½ 63V	35914
C514	22pF	PS	1pF 400V	39216
C515	.01µF	CE(2)	250V	22395
C516	.01µF	CE(2)	250V	22395
C517		PF	100V	37018
C518	33µF	E	16V	32173
C519	33µF	E	16V	32173
C520	33µF	E	16V	32173
C521	33µF	E	16V	32173
C522	.047µF	CE(2)	10V	19657
C523	47µF	T	16V	39215
C524	47µF	T	16V	39215
C525	.01µF	CE(2)	250V	22395
C526	33µF	E	16V	32173
C527	68pF	CE(2)		22374
C528	.01µF	CE(2)	250V	22395
C529				
C530	10µF	E	35V	32180
C531	10µF	E	35V	32180
C532				
C533	10µF	CE(2)	250V	22395
DIODES				
D501		1N4148		23802
D502		1N4148		23802
D503		1N4148		23802
D504		1N4148		23802
D510	2V7	ZENER		33921

OS4100 DISPLAY P.C.B. (Cont.)

Ref	Value	Description	Tol % ±	Part No
DIODES (Cont.)				
D511		1N4148		23802
D512		1N4148		23802
D513	2V7	ZENER		33921
INTEGRATED CIRCUITS				
IC501		µA356		39226
IC502		711		39227
IC503		µA356		39226
IC504		µA356		39226
IC505				
IC506		741		36736
IC507		AD561		39213
IC508		1408-L8		35683
IC509		74LS00		36730
IC510		74LS00		36730
IC511				
IC512		74LS175		36728
IC513		74LS161		36727
IC514		74LS175		36728
IC515		74LS112		36468
IC516		74LS175		36728
IC517		74LS161		36727
IC518		74LS175		36728
SWITCHES				
S501				
S502				39308
S503				
S504				
S505				
				39307
S507				
S508				
S509				
S510				39306
S511				
S512				
MISCELLANEOUS				
TR501		BC182B		33205

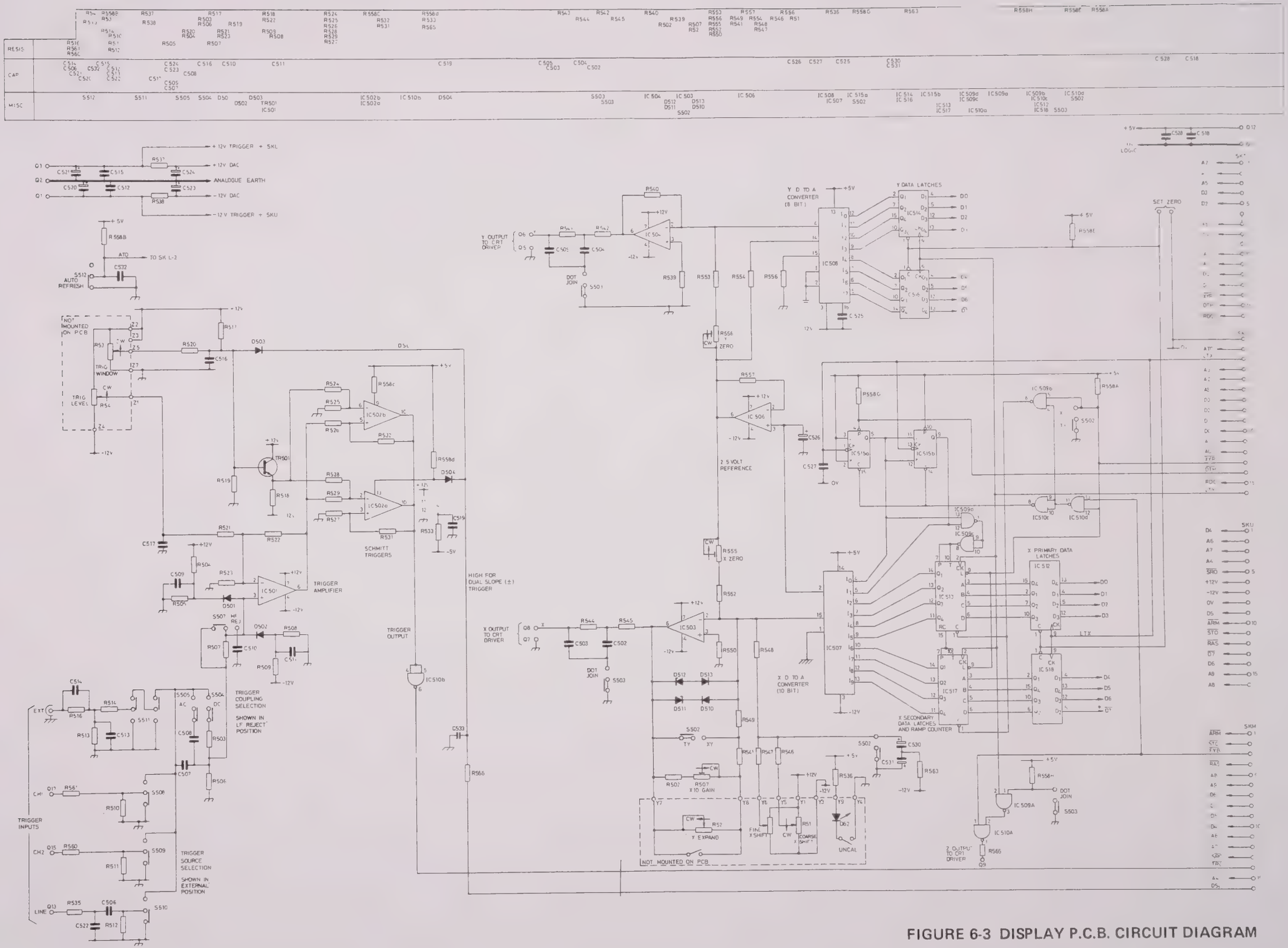


FIGURE 6-3 DISPLAY P.C.B. CIRCUIT DIAGRAM

OS4100 POWER SUPPLY

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R300	4M7	CF		30759
R400	1M	PCP		37539
R401	100k	CP		A4/39319
R402	1M	PCP		37539
R403	100k	CP		A4/39319
R404	4k7	PCP		37537
R405	470k	CF	5 ½W	18582
R406	1M8	MG		35752
R407	330	CF		28721
R408	33k	CF		21814
R409	1M5	CF	5 ½W	18588
R410	1k	CF		21799
R411				
R412	1M	PCP		39322
R413	200k	PCP		39264
R414	10k	PCP		39265
R415	100k	CP	5 ⅛W	21819
R416	24k	MF	2	38627
R417	82	CF		28717
R418				
R419	100	CF		21794
R420				
R421	100	CF		21794
R422	39k	CF		28728
R423	68k	CF	½W	18572
R424				
R425	4k7	CF		21805
R426	100k	CF		21819
R427	10k	CF		21809
R428	10k	CF		21809
R429	56k	CF		28729
R430				
R431	39k	CF		28728
R432	68	CF		28716
R433	150	CF		28719
R434	180	CF		21795
R435	390	CF		28722
R436				
R437	10k	CF		21809
R438	1k	MF	0.5	39463
R439	220	CF		21796
R440				
R441	1k	CF		21799
R442				
R443	22k	CF	1W	19053
R444	3k3	CF		21803
R445	2k7	MF	2	38604
R446	8k2	CF		21808
R447	270	CF		28720
R448				
R449	200	PCP		39231
R450				
R451				
R452	4k7	CF		21805
R453	10k	CF		21809
R454	220	CF		21796
R455	2k7	CF	2 ¼W	38604
R456	2k2	CF		21802
R457	1k	PCP		39233
R458	22k	CF	1W	19053
R459	3k3	CF		21803
R460				
R461	1k	CF		21799
R462	36k	MF	2	38631
R463				
R464				
R465				
R466	10k	CF		21809
R467	10	CF		21793
R468	220	CF		21796
R469	1k	CF		21799
R470				
R471	20k	PCP		39235
R472	22k	CF	1W	19053
R473	3k3	CF		21803
R474	2k7	MF	2	38604
R475	100	CF		21794
R476	47k	CF		21815
R477	47k	CF		21815
R478				
R479	100	PCP		39230
R480				
R481				
R482	10k	CF		21809
R483	220	CF		21796
R484	2k7	MF	2	38604
R485	22k	CF	5 1W	19053
R486	3k3	CF		21803
R487	1k	CF		21799
R488	10	CF		21793
R489	10M	CF	10	32661
R490				
R491	10M	CF	10	32661
R492	4k7	CF		21805
R493				
R494	470	CF		21797
R495				
R496	150k	CF		21821
CAPACITORS				
C300	500pF	CE(2)	10kV	31239
C301	.047μF	PE	1.5kV	36633
C302	3000pF	CE(2)	2kV	34381
C303	3000pF	CE(2)	2kV	34381
C304	3000pF	CE(2)	2kV	34381
C400	0.1μF	PF	100V	37018
C401				
C402	3000pF	CE(2)	3kV	34381

OS4100 POWER SUPPLY (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont.)				
C403	4.7µF	T	35V	53249
C404	270pF	CE(2)	500V	22380
C405	.01µF	CE(2)	250V	22395
C406	1500pF	CE(2)	63V	35919
C407	0.1µF	PF	100V	37018
C408	150µF	E	16V	32175
C409	1µF	E	250V	39327
C410	1000pF	CE(2)		22387
C411	150µF	E	16V	32175
C412	1µF	E	250V	39327
C413	.01µF	CE(2)	250V	22395
C414	56pF	CE(2)		22373
C415	0.1µF	PF	100V	37018
C416				
C417	0.1µF	PF	100V	37018
C418	1000pF	CE(2)		22387
C419	10000pF	PS	63V	35924
C420	2.2µF	E	53V	32194
C421	0.1µF	PF	100V	37018
C422				
C423	56pF	CE(2)		22373
C424	0.1µF	PF	100V	37018
C425	0.1µF	PF	100V	37018
C426	0.1µF	PF	100V	37018
C427	0.1µF	PF	100V	37018
C428	4700µF	E	25V	39330
C429	4700µF	E	25V	39330
C430	6800µF	E	16V	A4/39329
C431	6800µF	E	16V	A4/39329
C432	4.7µF	T	35V	53249

Ref	Value	Description	Tol %±	Part No
DIODES				
D300		HS2-4	3kV	39325
D301		HS2-4	3kV	39325
D302		HS2-4	3kV	39325
D303		HS2-4	3kV	39325
D400	100V	ZENER		37557
D401		1N4148		23802
D402	100V	ZENER		37557
D403		1N4148		23802
D404		1N4148		23802
D405		1N4936		39324
D406		1N4148		23802
D407	5V1	ZENER		33928
D408		1N4148		23802
D409	5V6	ZENER		33929
D410		1N4003		23462
D411		1N4003		23462
D412		1N4003		23462
D413		1N4003		23462
D414		1N4003		23462
D415		1N4003		23462
D416		1N4003		23462
D417		1N4003		23462
D418		1N4003		23462
D419		1N4003		23462
D420		1N4003		23462
D421		1N4003		23462

TRANSISTORS		
TR400	BC182	33205
TR401	BC212	29327
TR402	BFX88	23337
TR403	BC182	33205
TR404	2N5831	33209
TR405	BC212	29327
TR406	MJE3055	28770
TR407	BF258	31490
TR408	BC212	29327
TR409	BC182	33205
TR410	BC212	29327
TR411	BF258	31490
TR412	BC212	29327
TR413	BC182	33205
TR414	BF258	31490
TR415	BC212	29327
TR416	BC182	33205
TR417	BF258	31490
TR418	BC212	29327
TR419	BC182	33205

INTEGRATED CIRCUITS		
IC400	555	36813
IC401	709	40179
IC402	78M12	37259
IC403	78M12	37259
IC404	7805	36176
IC405	7805	36176
IC406	78L12A	40714
IC407	78L62A	36959

MISCELLANEOUS			
L400	330µH		40713
L401	330µH		40713
L402	330µH		40713
L403	330µH		40713
SCR400		2N5060	39328
BR400		W02	19725
BR401		W02	19725
V40		C.R.T. Thorn D14-182-GH-98	40022

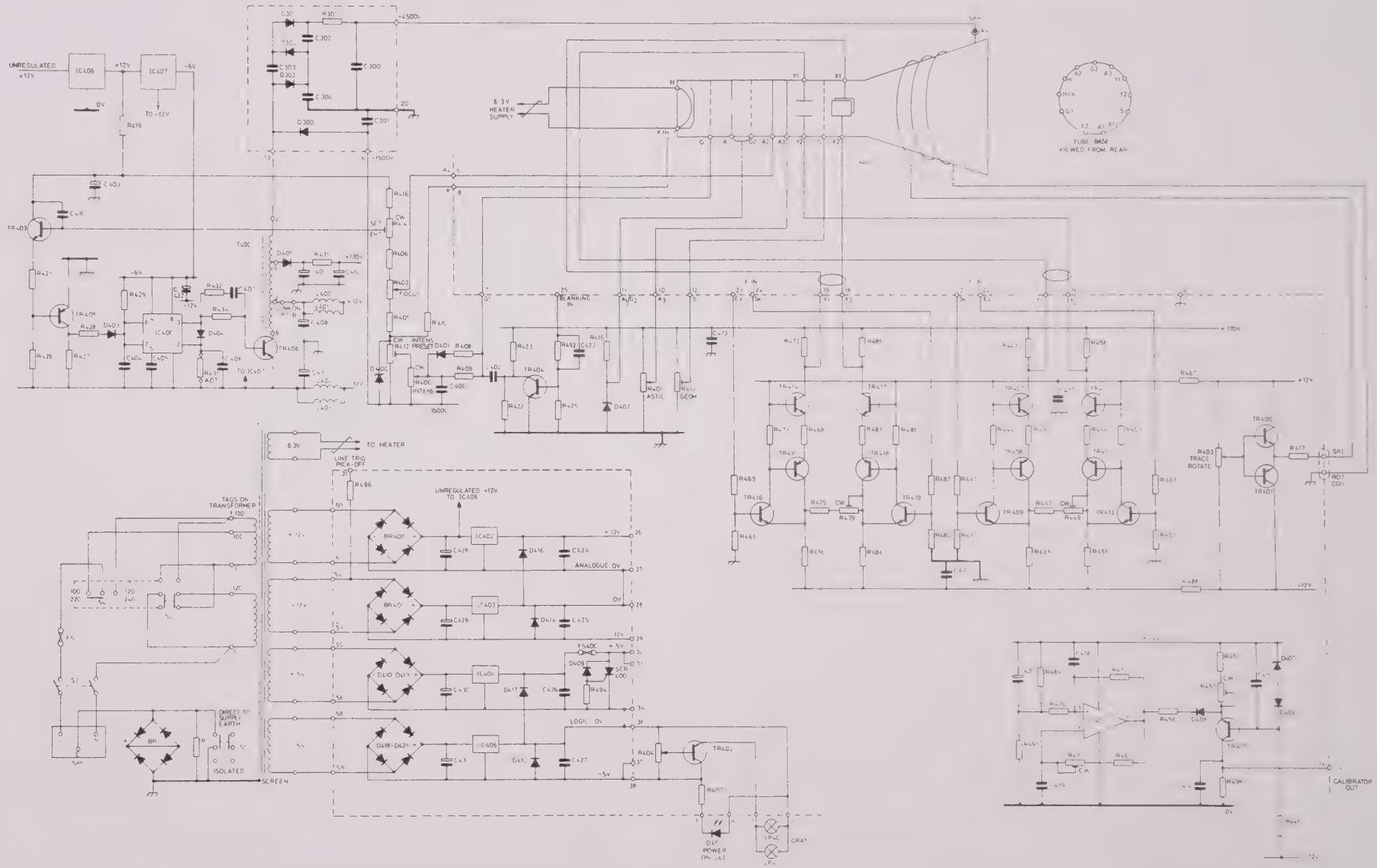


FIGURE 6-4 POWER SUPPLY CIRCUIT DIAGRAM

OS4100 INTERCONNECTIONS

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R1	100k	CF		21819
R10	2k2	CP with S14		A4/39256
R11	900k	MF	½	31929
R12	990k	MF	½	31927
R13	2k7	CF see drawing AO/SK 2576		28726
R14	47	CF see drawing AO/SK 2576		28714
R15	330	CF see drawing AO/SK 2576		28721
R16	100	PCP see drawing AO/SK 2576		39263
R17	100k	CF A.O.T.		21819
R18	10k	CF		21809
R19	82k	CF		21818
R20	2k2	CP not shown with S14		A4/39256
R21	900k	MF not shown	½	31929
R22	990k	MF not shown	½	31927
R23	2k7	CF see drawing AO/SK 2576		28726
R24	47	CF see drawing AO/SK 2576		28714
R25	330	CF see drawing AO/SK 2576		28721
R26	100	PCP		39263
R27	220k	CF		21823
R28	10k	CF		21809
R29	120k	CF		21820
R51	10k + 22k	CP		A4/39316
R52	10k	CP		A4/40000
R53	22k	CP		A4/39317
R54	22k	CP		A4/39317
R81	100k			A4/39412
CAPACITORS				
C10	5.6pF	CE(2) see drawing AO/SK 2576		22361
C11	.1μF	PE	500V	22363
C12	8.2pF	CE(2)		22366
C20	5.6pF	CE(2) see drawing AO/SK 2576		22361
C21	.1μF	PE	500V	22363
C22	8.2pF	CE(2)		22366
DIODES				
D10				39884
D20				39884
D40				39884
D61				39884
D62				39884
D63				39884
D64				39884
D65				39884
D66				39884
D67				39884
SWITCHES				
S1				24545
S3				24545
S4				24545
S10				39252
S11, S12, S13				39305
S14		with R10		A4/39256
S20				39252
S21, S22, S23				39305
S24		not shown with R20		A4/39356
S50				
S61				A3/39943
S81				A4/33869
S82				39368
MISCELLANEOUS				
RN10				A3/39333
RN20				A3/39333
TR10		BC182B		33205
TR20		BC182B		33205
T1				A1/39160
BR1		VH148		36281
LP40				35471
LP41				35471

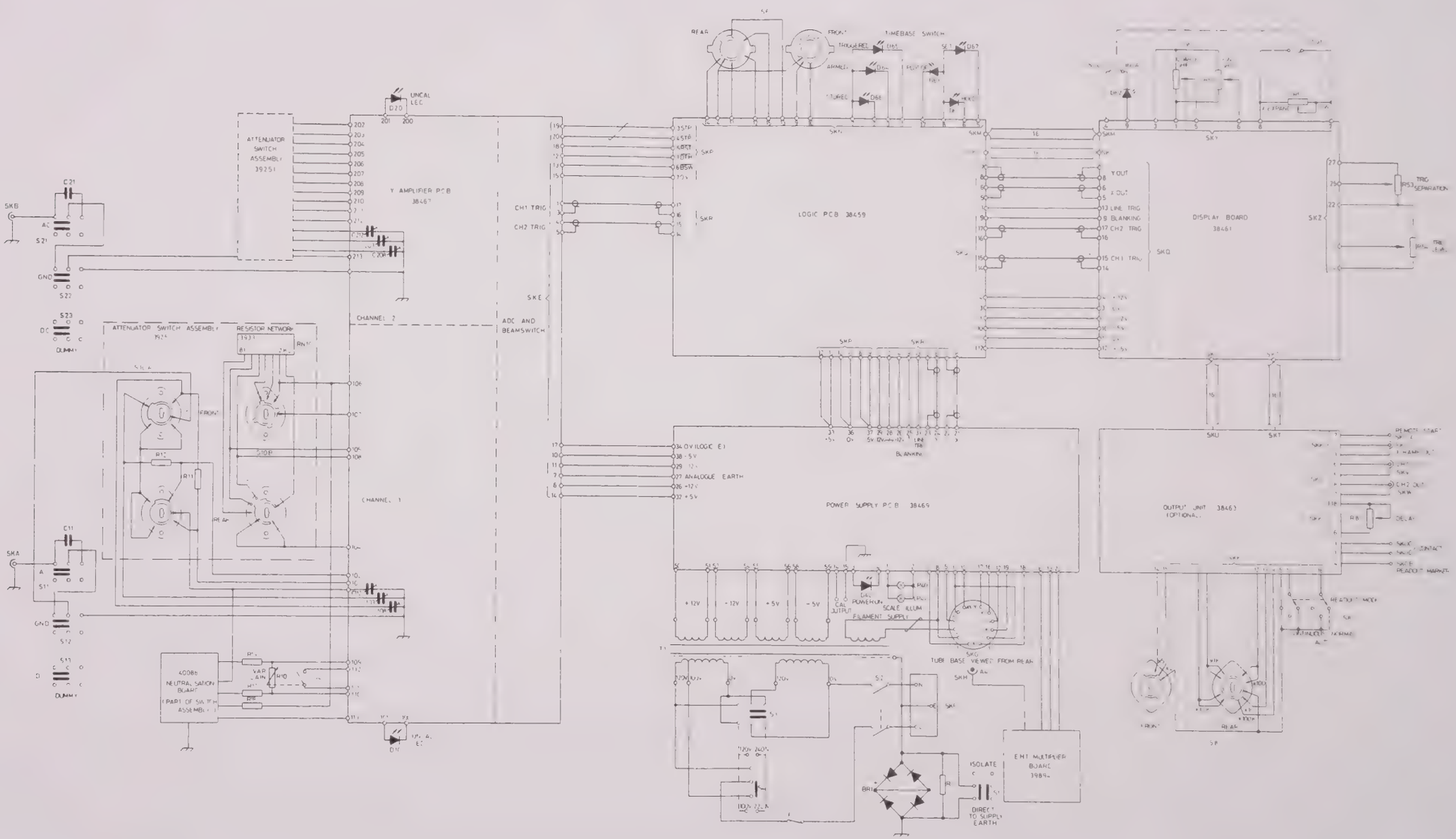


FIGURE 6-5 INTERCONNECTIONS CIRCUIT DIAGRAM

4103 OUTPUT UNIT

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R800	18k	CF		21811
R801	3k9	CF		21804
R802	4k7	CF		21805
R803	2k2	CF		21802
R804	2k2	CF		21802
R805	1k	PCP		39261
R806	200	PCP		40362
R807	100	CF		21794
R808	430	MF	2	38595
R809	430	MF	2	38595
R810	1k8	MF	2	38600
R811	1k1	MF	2	38595
R812	1k1	MF	2	38595
R813	100	CF		21794
R814	1k8	MF	2	38600
R815	430	MF		38585
R816	430	MF		38585
R817	1k1	MF	2	38595
R818	1k1	MF	2	38595
R819	2k7	CF		28726
R820	4k7 x 7	RESISTOR MODULE		40177
R821	430	MF	2	38585
R822	430	MF	2	38585
R823	10k	CF		21809
R824	10k	CF		21809
R825	100	CF		21794
R826				
R827	1k	PCP		39261
R828	200	PCP		40362
R829	20k	PCP		39229
R830	100	PCP		39263
R831				
R832				
R833	10k	CF		21809
CAPACITORS				
C80	0.1µF	CE(2)		36709
C81	0.1µF	CE(2)		36709
C82	0.1µF	CE(2)		36709
C800	.01µF	CE(2)	250V	22395
C801	.01µF	CE(2)	250V	22395
C802	.01µF	CE(2)	250V	22395
C803	.01µF	CE(2)	250V	22395
C804	2.2µF	T	35V	35930
C805	22µF	T	6V3	54230
C806	.01µF	CE(2)	250V	22395
C807	.01µF	CE(2)	250V	22395
C808	.01µF	CE(2)	250V	22395
C809	470pF	CE(2)		22383
C810	.01µF	CE(2)	250V	22395
C811	.01µF	CE(2)	250V	22395
C812	.01µF	CE(2)	250V	22395
C814	.01µF	CE(2)	250V	22395
C815	.01µF	CE(2)	250V	22395
C816	47µF	T	16V	39215
C817	47µF	T	16V	39215
C819	.01µF	CE(2)	250V	22395
C820	.01µF	CE(2)	250V	22395
INTEGRATED CIRCUITS				
IC800		74LS293		39241
IC801		74LS00		36730
IC802		74LS10		36867
IC803		74LS74		36732
IC804		74LS290		39240
IC805		74LS00		36730
IC806		74LS112		36468
IC807		74LS293		39241
IC808		74LS74		36732
IC809		74LS157		36735
IC810		74LS153		36247
IC811		74LS221		39239
IC812		74LS74		36732
IC813		74LS175		36728
IC814		74LS175		36728
IC815		74LS175		36728
IC816		74LS175		36728
IC817		MK5009		34952
IC818		74LS10		36867
IC819		AD561		39213
IC820		741		36736
IC821		1408/8		35683
IC822		741		36736
IC823		1408/8		35683
IC824		741		36736
IC825		741		36736
MISCELLANEOUS				
D800		1N4148		34701
TR800		B212		29327
RL800				36755
SKK				40017
SKS				37877
SKV				1222
SKW				1222
SKX				1222

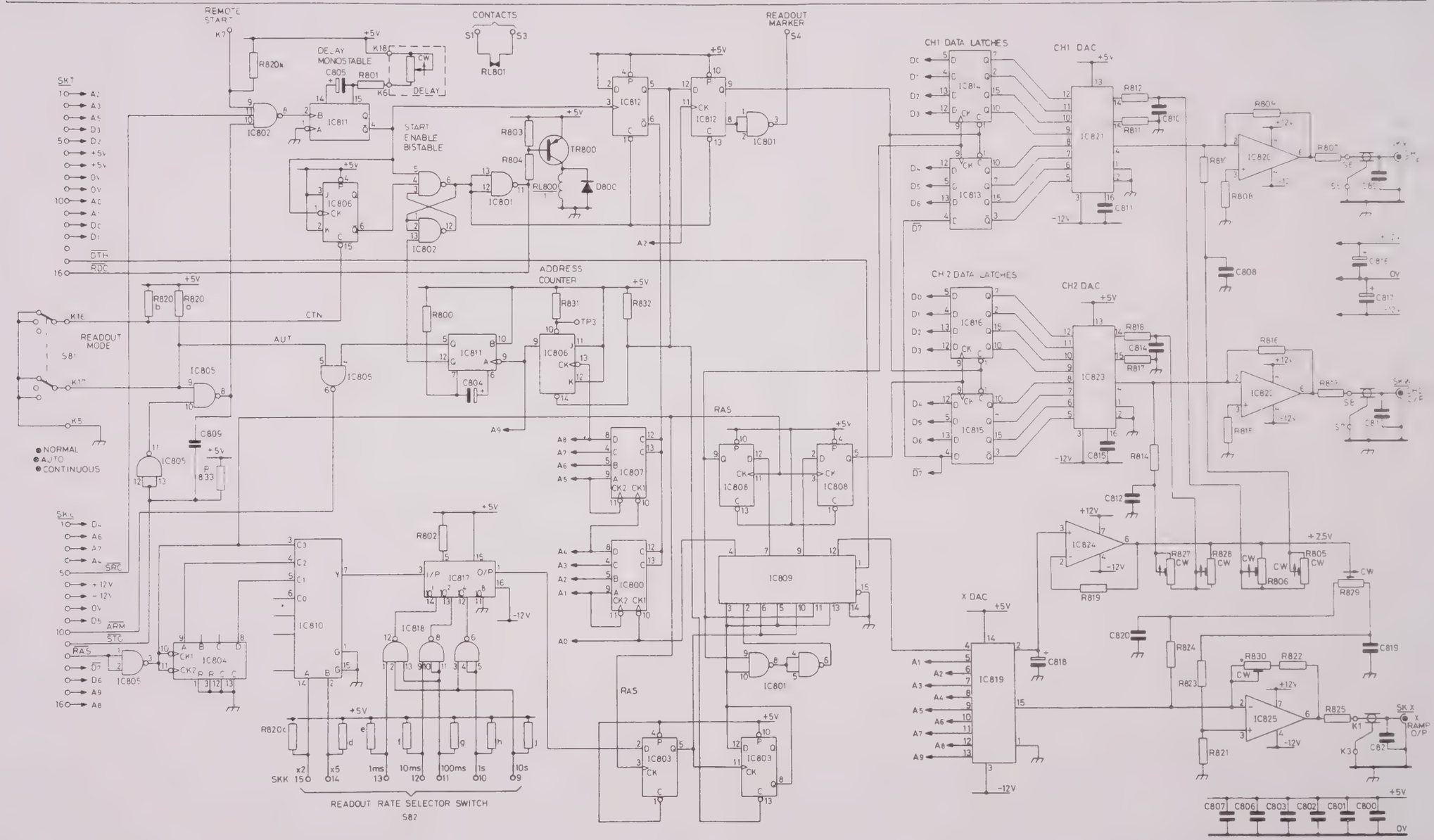


FIGURE 6-6 4103 OPTION OUTPUT UNIT CIRCUIT DIAGRAM

OS4100

ITEM No.	PART No.	DESCRIPTION
1	39863	Frame, Front & Rear
2	39828	Bulkhead R.H.
3	39829	Bulkhead L.H.
4	39830	Bracket Support
5	39821	Panel, Front
6	39822	Panel, Front
7	39824	Panel, Front, Outer
8	39827	Panel, Rear
9	39823	Panel, Front, Inner
10	39825	Panel, Front, Inner
11	35298	Moulding Tube Support
12	36351	Escutcheon
13	39832	Cover Top
14	39833	Cover Bottom
15	37864	Latch
16	37915	'O' Ring
17	39295	Handle Assy
18	39831	Screen Attenuator
19	39856	Cover C.R.T.
20	39890	Trim Side
21	39023	Spacer, Moulded
22	30578	Block, Indexing
23	36358	Spindle
24	29206	Spring
25	36681	Button, Handle
26	39837	Plate, Blanking
27	37721	Foot, Rear
28	32310	Binding Post
29	33787	Plug, Supply
30	39878	Bar Support Assy
31	39880	Bar Support Assy
32	39876	Bar Support
33	24159	Feed-Thro
34	39899	Pillar
35	39884	LED
36	38407	Knob (Push Button)
37	38408	Bezel (Push Button)
38	1222	Socket, BNC
39	25430	Skirt
40	25447	Cap (Red)
41	36337	Cap (LT. Parch.)
42	36332	Knob ($\frac{1}{4}$)
43	36333	Knob ($\frac{1}{8}$)
44	36336	Knob (4mm)
45	37698	Knob
46	25446	Cap (Red)
47	33071	Screw M3 x 12 C'sk Hd
48	22820	Screw 6-32 x $\frac{5}{8}$ Pan Hd
49	22817	Screw 6-32 x $\frac{5}{16}$ Pan Hd
50	1199	Washer 6-32 Plain
51	32626	Circlip
52	1200	Washer 4-40 Plain
53	22816	Screw 6-32 x $\frac{3}{8}$ Pan Hd
54	22843	Screw 4-40 x $\frac{5}{16}$ Pan Hd
55	22695	Screw 4-40 x $\frac{5}{16}$ Pan Hd Taptite
56	22842	Screw 4-40 x $\frac{1}{4}$ Pan Hd
57	36334	Knob($\frac{1}{4}$)
58	39883	Knob (6mm)

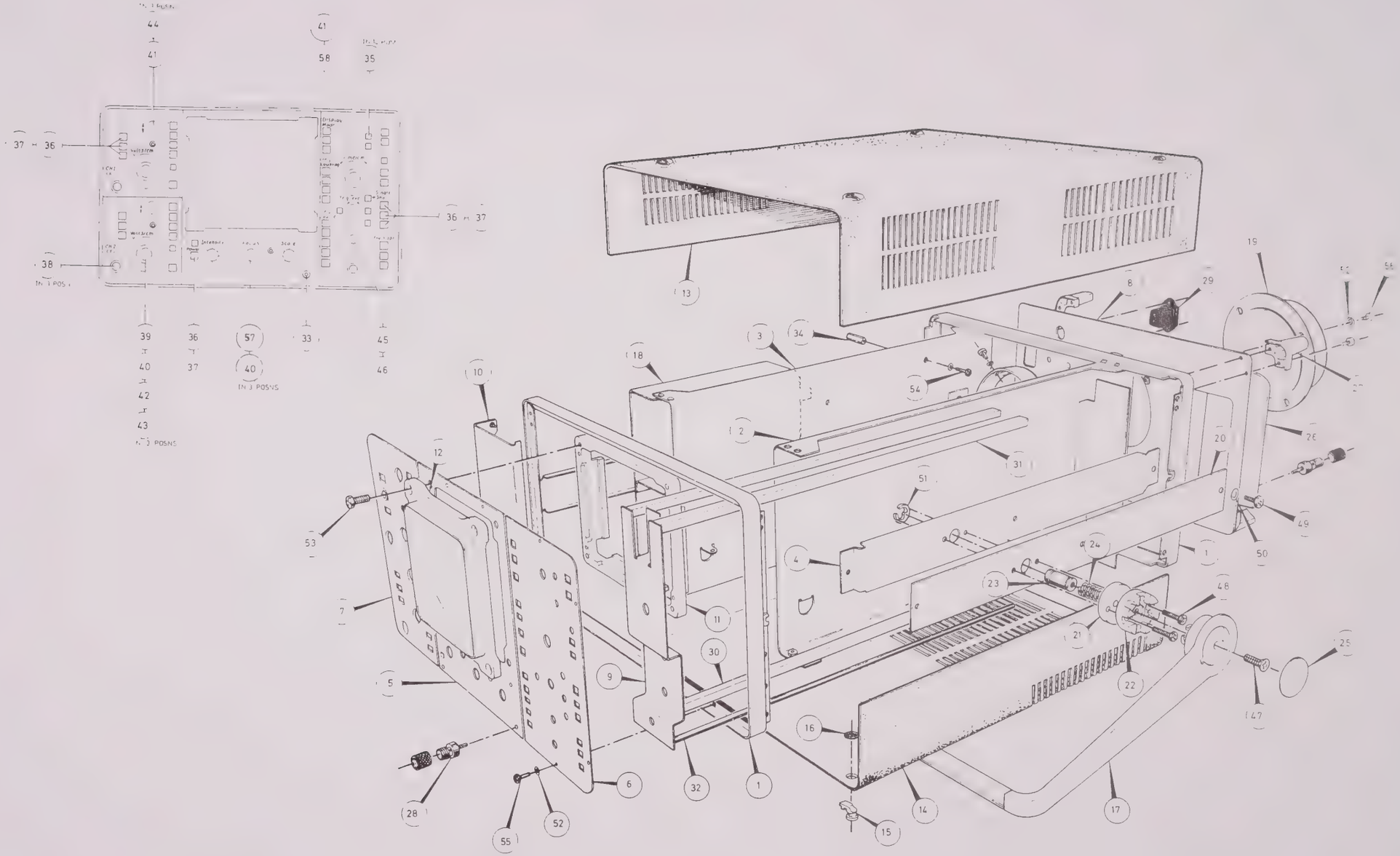


FIGURE 6-7 MECHANICAL VIEW

SECTION 7

WARRANTY AND SERVICE FACILITIES

Gould Oscilloscopes are warranted for a period of two years from date of shipment to original purchaser. They are warranted to conform to the applicable published specifications in effect at the time of shipment, and to be free from any defects in material or workmanship.

LIABILITY OF THE GOULD INSTRUMENTS DIVISION UNDER SUCH WARRANTY IS LIMITED TO SERVICING OR REPLACING DURING THE WARRANTY PERIOD AT THEIR OPTION, ANY DEFECTIVE PARTS EXCEPT COVERS, PROBES OR FUSES AND DOES NOT INCLUDE CALIBRATION AND MINOR MAINTENANCE AS OUTLINED IN OPERATING MANUALS. IN NO EVENT SHALL THE GOULD INSTRUMENTS DIVISION BE LIABLE FOR COLLATERAL OR CONSEQUENTIAL DAMAGES.

Units are to be returned transportation prepaid by the buyer. The Gould Instruments Division will have the right of final determination of the cause and existence of a defect under this warranty. This warranty shall not apply to any products which have been subjected to misuse, improper installation, repair, alteration, neglect, accident, inundation, fire or operation outside their published maximum ratings.

PACKING INFORMATION

If the unit is to be returned for service, it must be adequately packed as follows:

a) Seal the unit in an oversize plastic bag.

b) Pack the bagged unit into a heavy duty cardboard box. The box must have a minimum of 2 inches of cushioning on all six sides, so that the unit fits snugly.

c) Any accessories or instruction manuals must be sealed into a separate plastic bag and packed with a minimum of 2 inches of cushioning between the instrument and the accessories.

d) Before sealing the box with packing tape, ensure that an official packing note is inserted, giving full details of sender's name, address and telephone number, instrument type number and serial number, plus an indication of the reason for return, and/or fault conditions, if applicable.

e) Properly label and address the outside of the box.

f) Notify Gould in advance of shipment and ship prepaid by United Parcel Service or equivalent.

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Boston, MA
129 Middlesex Turnpike
Burlington, MA 01803
Phone: (617) 272-0750

Calgary, AB, CANADA
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Calgary, AB T2E625
Phone: (403) 230-1341

Cleveland, OH
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Cleveland, OH 44114
Phone: (216) 361-3315

Columbia, SC
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1201 St. Andrews Road
Columbia, SC 29210
Phone: (803) 798-8070

Dayton, OH
4668 Gateway Circle
Dayton, OH 45440
Phone: (513) 433-9605

Denver, CO
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Englewood, CO 80110
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Detroit, MI
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Southfield, MI 48075
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Elk Grove Village, IL 60007
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Ft. Lauderdale, FL 33309
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EMC Corporation
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Honolulu, HI 96819
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Saddle Brook, NJ 07662
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Lanham, MD 20801
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